SAMA5D3 Radiation Test Report

VERSION 01
RELEASED

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1   Document History

Please see the following record of revisions:

Document Revision	Document Status	Change Description
01	RELEASED	Initial revision post internal review.

2   References

The following references are applicable to this document.

Document Reference	Document Title	Date	Reference in this Document
SAMA5D3 Series Datasheet	Atmel-11121F-ATARM-SAMA5D3-Series-Datasheet_02-Feb-16	Feb 2016	[SAMA5D3 Datatsheet]

3 Introduction

One of the key components of the Open Source Satellite (OSSAT) command and data handling system is the microprocessor for the On Board Computer (OBC). Microprocessors that have been designed to be radiation-hardened for the harsh space environment are expensive and tend to have poor performance compared to Commercial-Off-The-Shelf (COTS) equivalents that leverage the latest innovations in microprocessor technology. The OSSAT team possesses decades of experience in using COTS components in Low Earth Orbit (LEO) and intends to leverage the capabilities of the latest terrestrial technology in the development of the OSSAT platform computer.

The OSSAT team performed a research and development project to further the understanding of COTS processors, in partnership with the Surrey Space Centre (SSC) at the University of Surrey, UK, with support from Research England's SPRINT programme[1]. The OSSAT-SSC project team evaluated the latest available COTS microprocessors[2] and assessed their suitability in terms of performance with a view to test their resilience to the harsh space radiation environment. Three COTS processors were downselected and subjected to a series of research tests to determine processor performance and space environmental resilience.

4 Scope

This document is the third and final in a set of three reports that present the results of the microprocessor research. Each document describes:

- The justified evaluation criteria for the selected processors.
- The key features of each processor.
- The results of the two types of tests performed on each processor:
  o A test of the processor's performance.
  o A test of the processor's susceptibility to the effects of the space radiation environment.

This third and final document gives the results of this research in relation to the third of the three downselected processors, the Microchip/Atmel SAMA5D3.

5 Processor Selection

5.1 Selection Criteria

Several quantitative and qualitative criteria were defined in order to evaluate a suitable microprocessor to integrate into the OSSAT platform. This section presents the criteria with justifications listed in descending order of importance.

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[1] https://sprint.ac.uk/about-us/
[2]   https://www.sprint.ac.uk/news-stories/kispe-space-joins-sprint-to-source-microprocessors-for-next-generation-microsatellite-platforms/

2

5.1.1   Performance Requirement

The **minimum** performance figure of **200 DMIPS** has been defined.

5.1.1.1   *Performance Requirement Rationale*

The OSSAT team has experience in working with OBCs for a wide range of different missions. We are aware of the increasingly demanding performance requirements that flight software places on OBCs for new and emerging mission needs. For example: higher Attitude and Orbit Control System (AOCS) algorithm execution rates (in the range of 4-12Hz to support increased agility), higher telemetry sampling rates (in the range of 20Hz to improve the speed of anomaly diagnosis) and larger files (log data will be plaintext in order to reduce the time required to interpret the data).

Our survey of commercially-available space OBCs identified products that have a performance of 50 to 60 DMIPS, which do not satisfy the performance criteria required to enable a new generation of space-enabled missions, applications and services. The 200 DMIPS represents a substantial improvement in this performance without a significant increase in power consumption.

The availability of a very high-performance platform processor can lead to a blurring of the boundary between platform and payload because of the temptation to embed payload operations within such a processor, potentially leading to complicated and blurred functionality. Our design philosophy is to maintain a platform-payload separation to eliminate the risk of mission-specific payload requirements driving changes and NRE on the platform design.

NOTE: The DMIPS measure takes no account of floating-point operations.

NOTE: Manufacturers often measure performance in units of either Coremarks or DMIPS. We adopted DMIPS because it seemed the most common measure. Where manufacturers gave measurements in Coremarks, we translated the figures approximately into DMIPS.

5.1.2   Power Consumption Requirement

The maximum amount of power consumed by the processor must **not exceed 300mW** at ambient temperature.

5.1.2.1   *Power Consumption Requirement Rationale*

Power consumption is always a principal consideration on space missions. The platform must consume as little power as possible in order to maximise the power available for payloads and thereby enhance mission utility. The OSSAT team intends to capitalise on advances in low power processing technology to identify potential options that satisfy this requirement. It is also important to recognise that, when conducting a paper exercise, power consumption figures quoted by manufacturers can be difficult to interpret. A pragmatic and appropriate level of effort was applied to ensuring that the comparison of power figures is fair.

5.1.3   Floating Point Operations Requirement

The processor must be capable of processing arithmetic on **floating point numbers**.

5.1.3.1 Floating Point Requirement Rationale

The platform processor will need to perform AOCS algorithms at relatively high speeds (more than 4 Hz and up to 12Hz). To code these algorithms in integer maths is not practical. The processor therefore needs to support floating point operations. NOTE: this can be achieved either through the integration of a floating-point unit or otherwise through a compiler that can translate from floating point to integer maths through the compilation process. In this case, the general performance figure should be increased. As a preference, the processor would have a floating point unit (single or double precision).

5.1.4   Program Memory Requirement

The processor must be able to address at least **50MB** of **program memory** (the non-volatile memory used to hold the program).

5.1.4.1 Program Memory Requirement Rationale

Programs are anticipated to be in the region of 100's of kilobytes rather than 50MB. For example, KISPE recently integrated FreeRTOS with a Board Support Package (BSP) and a number of tasks all compiled down to <200kB of Program data on an ARM Cortex-M7. However, other Linux-based operating systems, that potential OSSAT users may wish to implement, have a much bigger footprint. Also, the introduction of run time uploadable tasks may result in far less efficient use of program memory. 50MB provides capacity to accommodate a wide range of programs. NOTE: This memory can be on-chip or off chip (with a preference for on chip so long as it has Error Correcting Code (ECC) protection).

5.1.5   Data Memory Requirement

The processor must be able to address at least **64MB** of **data memory** (the volatile memory used by the program during execution).

5.1.5.1 Data Memory Requirement Rationale

There are a number of consumers of data memory, including:

- Buffering data destined for the file system, depending upon file system performance, this may be significant.
- Buffer I/O.
- Data structures for the RTOS.

The OSSAT team have recently integrated FreeRTOS with a BSP and a number of tasks, all compiled down to use <400kB of data memory that was statically allocated). The amount of required memory may vary greatly and therefore 64MB was defined to address anticipated needs.

NOTE: This memory can be on-chip or off chip. Ideally, this memory would be on chip and with ECC protection.

5.1.6   Mass Memory Requirement

The processor must be able to accommodate at least **4GB** of **mass memory** to house the file system.

5.1.6.1   *Mass Memory Requirement Rationale*

Platform telemetry data will be stored alongside operational timetables that schedule activities and configuration files. This data will be stored in a file system that is housed on a mass memory. The mass memory should ideally be non-volatile so long as the file integrity can be maintained in environments susceptible to Single Event Upsets (SEUs). Some non-volatile memory needs to be baselined since the spacecraft configuration will be stored in a memory that needs to survive power interruptions and resets.

5.1.7   Thermal Requirement

The processor must be able to fully operate between -40 to +85 degrees C.

5.1.7.1   *Thermal Requirement Rationale*

This temperature range covers the majority of operating temperatures that will be experienced by the spacecraft. It is also the typical range for the majority of automotive electronic components that are being considered for OSSAT, giving the maximum flexibility to the thermal design of the spacecraft.

5.2   Qualitative Criteria

A number of other features and properties are relevant to the platform processor selection, including:

5.2.1   External Memory Interfaces

SEU memory protection can be implemented off-chip in hardware if the chip supports external memory interfaces.

5.2.2   Existing Radiation Tolerance data

Any existing data about the radiation tolerance of the processor would be beneficial. Furthermore, some parts have pin compatible radiation tolerant equivalents. These parts are potentially more relevant because the radiation tolerant equivalent part could be used for "beyond LEO" missions without needing to re-engineer these core elements of the platform software or PCB layout.

5.2.3   Existing SEU Protection

As the feature size of components has reduced, commercial processors have become susceptible to SEUs even when used in terrestrial applications. Therefore, some vendors have introduced error detection or error detection and correction technology into the silicon. Availability of SEU mitigation, such as single bit per word error detection and correction, is an important consideration.

5.2.4   Development Tool Compatibility

The availability of tools to aid the development of software for the processor and to model power consumption was considered, as was whether the tools are open source, whether support is available for a fee, and how large the userbase is.

5.2.5   RTOS availability

The quantity of Real Time Operating Systems (RTOS's) that support the processor was assessed, as was whether the RTOS's are open source.

5.2.6   Field-Programmable Gate Array (FPGA) configurability

FPGAs offer an extra degree of reconfigurability. FPGAs with embedded processors were therefore preferred and any FPGA hardware noted during the selection.

5.2.7   Cyclic Redundancy Check (CRC) Generation

Existence of hardware acceleration of CRC generation was evaluated because CRC generation will be a common task of the platform processor. It should be noted that the use of CRC protection should be weighed up against error detection and correction for communications interfaces.

5.2.8   Encryption/Decryption AES256

Existence of hardware acceleration to aid cipher/decipher was evaluated in order to satisfy the requirement for encryption to AES256: NOTE: the adoption of encryption must be weighed against power consumption, message sizes and the resulting effect on bit error rate.

5.2.9   Authentication (e.g. SHA-1)

Whether or not the processor includes hardware acceleration that aids authentication was assessed. This was considered because communications with the ground will need to be authenticated.

5.2.10 Flight Heritage

Previous in-orbit data, and information on the type of mission, if available, was evaluated.

5.2.11 Obsolescence

Production runs of components can be very short. This largely depends upon the industry for which the processor is manufactured. Chips manufactured for the automotive and aerospace industries are attractive because of the very long production runs, allowing the same components to be used across a series of different missions without needing to redesign the system.

5.2.12 Interfacing

The types and quantities of I/O interfaces that are supported by the chip was considered. Should specific technologies not be supported by the chip, supplementary devices could be used to provide the required interface.

5.3   SAMA5D3 Specification (Part # ATSAMA5D35A-CN)

This is a high performance processor that can achieve 800 DMIPS whilst consuming a low amount of power. It incorporates an ARM A5 32 bit core (see [SAMA5D3 Datatsheet]). It has a strong capability with respect to memory interfacing, including a static memory controller with built in ECC. This processor has been baselined for a few space missions include AAReST and at least one Cubesat mission.

Criteria	Target	Actual	Supplementary Circuitry required
Performance	200 DMIPS	825 DMIPS[3]	N/A
Power Consumption	300mW	336mW during radiation test NOTE: During the paper evaluation, power analysis showed this chip consuming 150mW but the actual (test) value was 336mW	N/A
Floating Point	FPU desirable	Double Precision FPU	N/A
Program Memory	50MB	160kB (internal) – cannot be reprogrammed from a factory delivered bootloader	External program memory
Data Memory	64MB	128kB(internal)	External data memory
Mass Memory	64GB	None (other than the data memory already mentioned)	Lots of options for external memory including ECC protection. NOTE: If chosen: SD/MMC memory can be used but incorporates very high memory densities. This presents a risk (small transistor sizes could SEU easily & memory could be slow).
Thermal	-40 to +85 degrees C	-40 to +105 degrees C	N/A

The outcome of the chip against the qualitative criteria is as follows:

Criteria	SAMV71 capability
External memory interfaces	There are plenty of options including a static memory controller with built in ECC, up to 512 Mbytes of SDRAM are addressable, up to 1GByte

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[3] This assumes the cache memory is enabled.

Criteria	SAMV71 capability
	SRAM/Flash can also be addressed. SD card interfacing is also possible
Existing radiation tolerance data	None found.
Existing SEU protection	ECC protection as part of the NAND Flash static memory controller which interfaces to external static memory. This can correct either 2, 4, 8, 12 or 24 errors per sector depending upon sector size. Processor cache is unprotected.
Development tools	FreeRTOS, Linux, GNU compilers, assemblers, linkers, GDB including a processor simulator. The tools have a very wide userbase (particularly the GNU toolchain). Support is not payable unless you purchase a commercial toolchain (IAR/Keil). There appeared to be no power modelling tools available for this chip.
RTOS availability	FreeRTOS and other commercial alternatives.
FPGA configurability	This chip is not included within an FPGA; however an external FPGA could be incorporated in the platform computer design.
CRC Generation	No general-purpose hardware acceleration. OSSAT will need to perform CRC computations on general memory (for comms protocol for example), this will need to be implemented in software on this chip.
Encryption/Decryption	AES 128/192/256 h/w acceleration is part of the chip.
Authentication	SHA1, 224, 256, 384, 512 h/w acceleration is part of the chip.
Flight Heritage	Baselined for a few missions (ARReST and a cubesat mission) and also PyCubed-1 (University project).
Obsolescence	This chip is designed for the IoT wearables market. This is a high turnover market that could present a risk in terms of obsolescence. The SAM series chips are very popular generally and production runs are likely to run for many years.
Interfaces	1 * ITU-R BT. 601/656 Image Sensor Interface 3 * HS/FS/LS USB Ports with On-Chip Transceivers 1 * One 10/100/1000 Mbps Gigabit Ethernet Media Access Controller (GMAC) with IEEE1588 support 1 * 10/100 Mbps Ethernet Media Access Controller (EMAC) 2 * CAN Controllers 1 * Softmodem Interface 3 * High Speed Memory Card Hosts (SD card/eMMC)

Criteria	SAMV71 capability
	2 * SPI 3 * I2C 6 * UARTS 2 * 3-channel 32-bit timer/counters 1 * 4-channel 16-bit PWM Controller 1 * 12 channel ADC. NOTE: this chip is a little more limited in terms of I/O interfacing than others. This means that this chip is less suited to directly interface to AOCS sensors and actuators should this be required.

5.4 Evaluation Summary

The SAMA5D3 matches the defined evaluation criteria well from the perspective of power consumption, run-time processor power, floating point support and external memory interfacing. Apart from memory interfacing, its I/O interfacing is a little more limited than other chips that have been evaluated.

6 SAMA5D3 test results

Following the down-selection of this chip, the following tests were performed using evaluation hardware.

6.1 Total Ionising Dose Radiation Test

6.1.1 Test Setup

6.1.1.1 Test Facility

The Realistic Electron Environment Facility (REEF), located at the University of Surrey, UK, and operated by research colleagues from SSC exposes samples in vacuum to a ~2.5 GBq Sr-90 source. Strontium-90 provides an excellent practical option for the provision of long-duration, low-intensity exposures as it allows uninterrupted irradiations over the required long periods with an electron spectrum that is appropriately representative of the real space environment.

Figure 1: REEF equipment at the University of Surrey

The REEF can be used to test materials and components for their vulnerability to both internal charging and total ionising dose phenomena. The dose rate is proportional to electron current and thus is primarily determined by the source-to-sample separation distance in the experimental setup. Changes to the electron spectrum change due to component shielding. This was taken into account (see section 6.1.4.1).

The dynamic range of normal incident electron current achievable with REEF is wide, ranging from ~6 pA/cm^2 at low (~3.5 cm) source-sample separation to ~0.3 pA/cm^2 at high source-sample separation (~16 cm). Higher currents can in theory be achieved at even smaller separations, though this would be at the expense of the assumption of normal incidence irradiation. Further reductions in current are achieved by adding planar aluminium shielding in between the source and sample.

The processor components to undergo testing were exposed to radiation equivalent to a 10 year, 800km, sun synchronous LEO mission. Upon completion of the REEF test for each board, any boards that showed forms of damage were tested again outside REEF to test for any potential annealing effects following irradiation.

6.1.2   The Target Under Test
In order to generate statistically relevant information, four SAMA5D3-Xplained evaluation boards featuring the downselected chip (the "Target") were irradiated.

Figure 2: SAMA5D3-Xplained Eval Board: Image Credit: Microchip/Atmel

The intent of the test was to assess the radiation tolerance of the processor only, therefore the rest of the components were shielded from the radiation source.

Each evaluation board was placed inside REEF and the radiation source positioned in order to test at a 1 kRad/hr dose rate as shown in Figure 3.
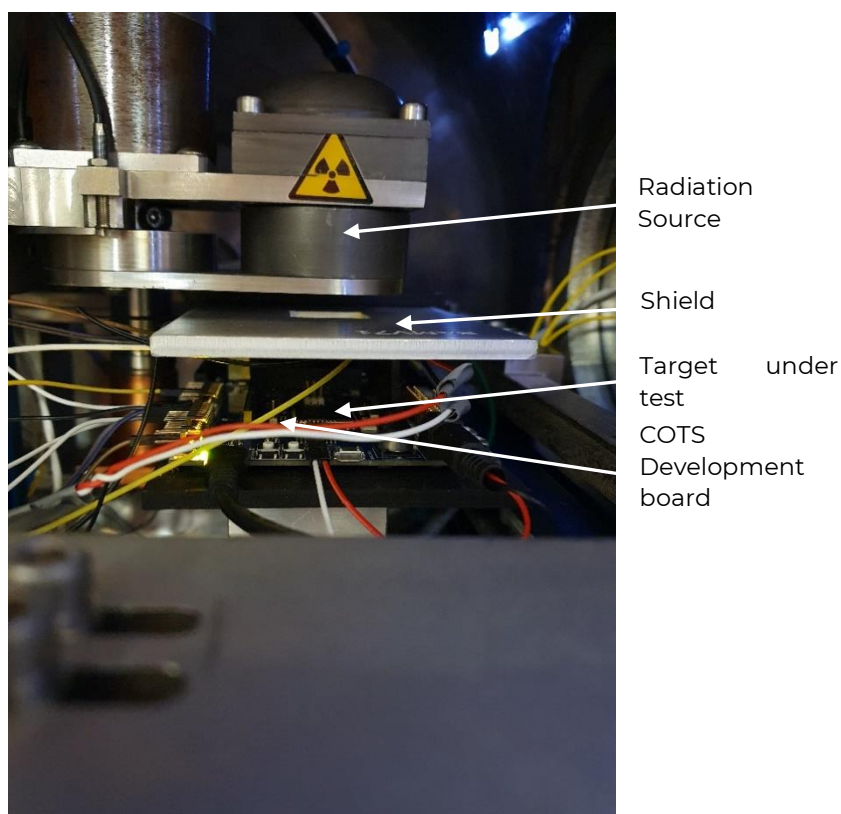

Figure 3: SAMV71 inside REEF

6.1.2.1 Target Software

The target processor was powered during irradiation. It ran software exercising various I/O interfaces and memories. The Test cycle repeated autonomously as illustrated in Figure 4 (NOTE: the wait between tests was reduced to 3 seconds in contrast to this figure. The original rationale for 30 seconds related to the anticipated time required to ensure a current & voltage measurement during the test. However, the current and voltage measurement mechanism proved faster than anticipated).
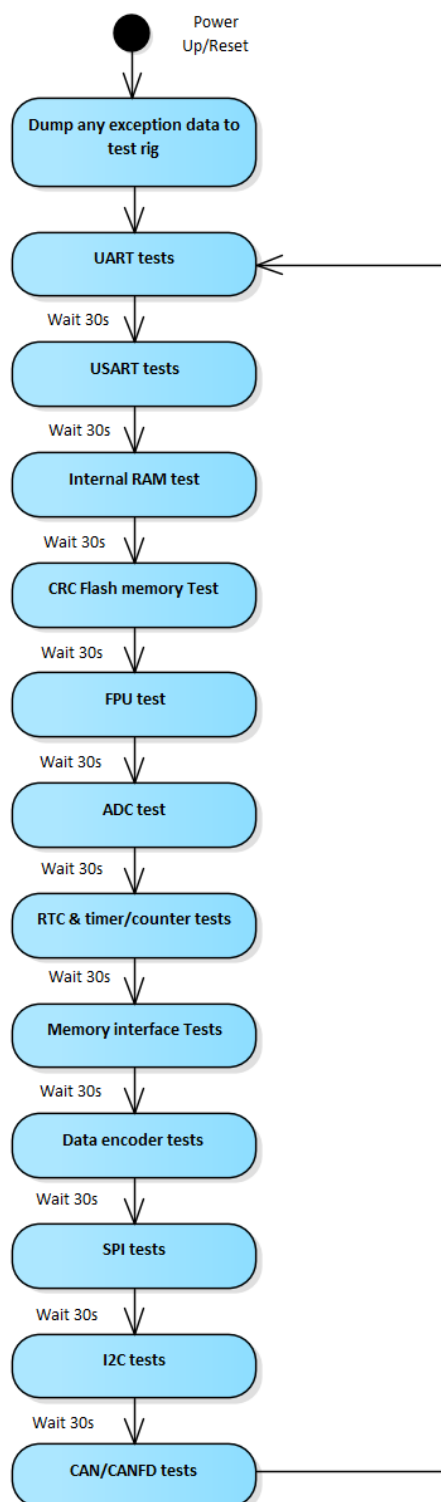
Figure 4: Test software loop

The tests were as follows:

- The I/O test for UART and USART test included signalling at the physical layer which were looped back so that both transmission and reception were tested.
- The on chip RAM was tested using a scrub, read, write method.

- The Floating Point Unit was exercised using a ray tracing algorithm.
- ARM exception handlers were written to output the value of the exception registers should exceptions occur during code execution.
- NOTE: Time did not allow for the development of software to support the testing of the Real Time Clock, the timers, counters, AES encoder/decoder, ADC, I2C, SPI and ECC. Tests were limited to those that were considered essential. This specific chip does not have an internal flash that can be reprogrammed. Therefore, the CRC Flash memory test was omitted.

All of the above tests and exception handlers output data were sent across both a CAN bus and a UART to a test PC that collated the information.

6.1.3 Test Rig Setup

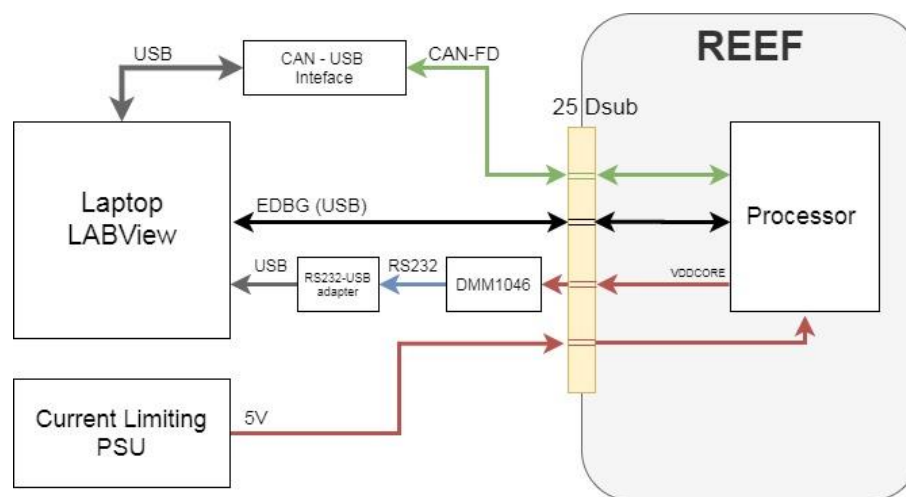The test rig setup is illustrated as shown below.

Figure 5: REEF Test rig setup

Test data was transmitted via two channels:

- A UART that the SAMA5D3-Xplained multiplexes into a USB channel using Atmels EDGB interface.
- A Controller Area Network (CAN bus).

Two dissimilar communications channels were chosen in order to mitigate the possibility that the radiation dose affected one of these channels but not the rest of the chip under test. A test was also conducted of the CAN bus integrity (to ensure that the SAMA5D3 CAN controller was functioning correctly). This CAN test involved both transmission and reception of CAN data to and from the target.

Alongside the above tests, the current and voltage to the chip under test was monitored using a Digital Multi Meter (DMM).

All of the above data was captured to a comma separated text file alongside the current radiation dose using a LABView program that interfaced to the DMMs, the CAN bus and the UART (through EDGB). The LABView program also incorporated a Graphical User Interface (GUI) that gave real time feedback to an operator. The GUI is shown below.
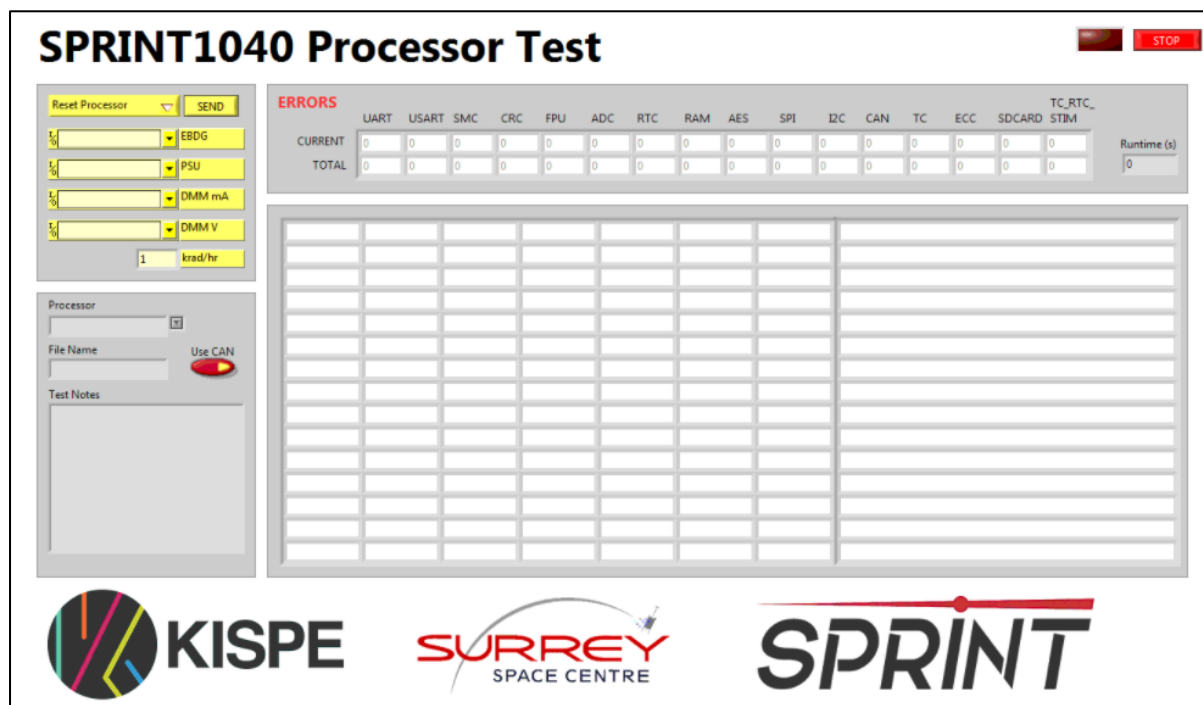
Figure 6: REEF Test Rig Utility GUI.

Testing was automated such that the system automatically attempted to resolve errors by resetting the peripheral causing the error using a stepped approach such as illustrated for the I/O tests in Figure 7. This involved a combination of functions on the target (highlighted blue) and functions of the test rig utility (highlighted red). The number of failures were held in a non-volatile memory (SD card) such that the progression through the failures was maintained by the target through power cycles of the target.
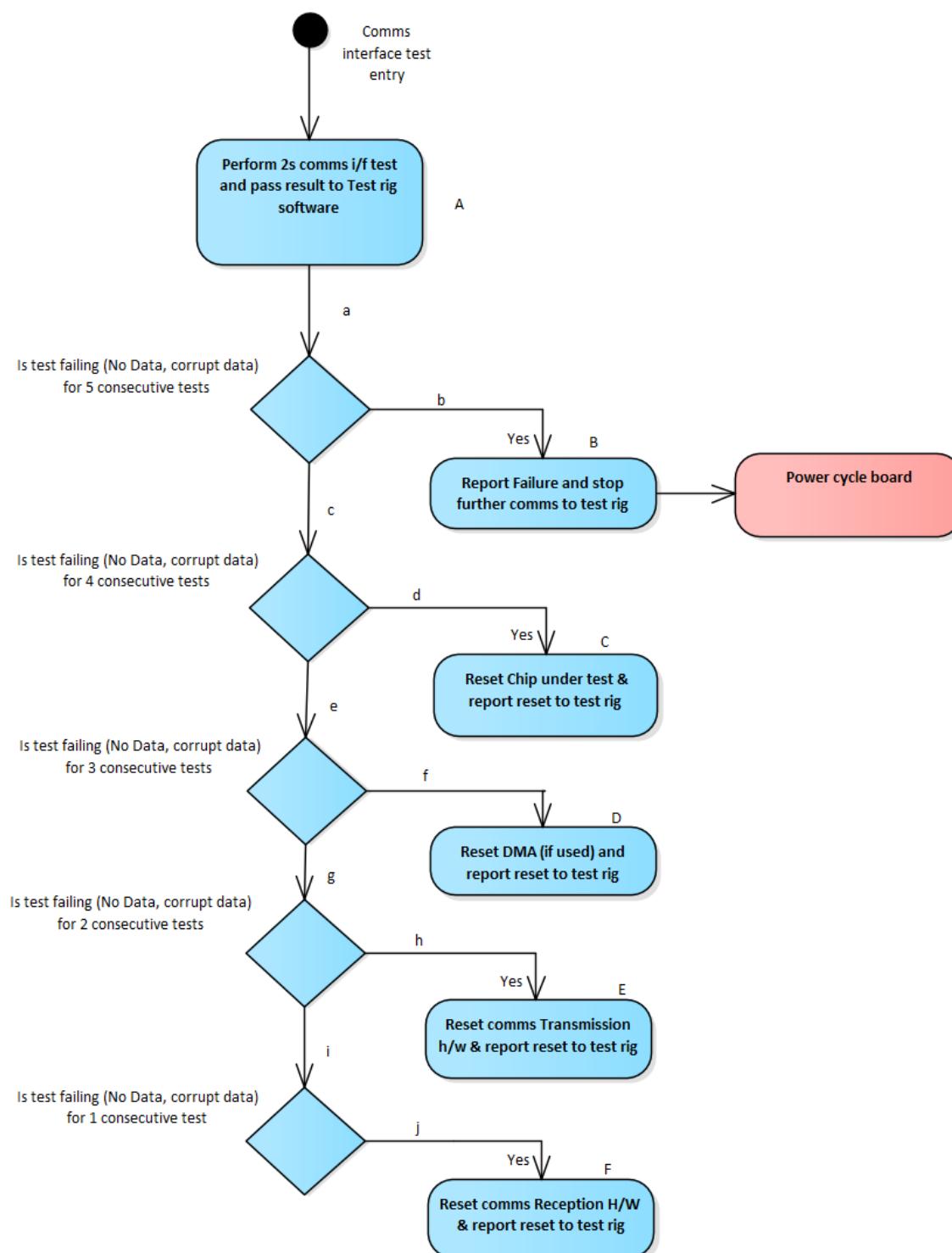
Figure 7: Automatic recovery from I/O interface errors

This mechanism allowed the tests to be conducted without operator interaction which allow the tests to run whilst being compliant with COVID-19 restrictions applied by the University of Surrey during 2020 and 2021.

6.1.4 Test Analysis

This section summarises the radiation environment calculations used to plan the experimental work for test board irradiations in REEF. The expected total ionising dose (TID) over the course of a nominal mission, and the dose rate within the test facility at the University of Surrey were calculated.

6.1.4.1 ORBIT ANALYSIS

The Space Environment Information System (SPENVIS) was used for both the radiation environment specification (trapped protons, trapped electrons and solar protons) and the dose-depth calculations. The following inputs were used:

- 800 km sun synchronous orbit
- 10 year mission duration
- Standard trapped environment models AE8 and AP8
- SAPPHIRE solar proton model (at 90% confidence over 10 year mission duration)
- SHIELDOSE-2 used for dose-depth with planar shielding geometry
- Spacecraft shielding assumed to be 2mm

Trapped proton and electron fluxes in the Van Allen belts were calculated via SPENIVS using the standard AE8 and AP8 environment models. Figure 8 shows example integral flux maps above 2 MeV and 10 MeV for electrons and protons respectively.
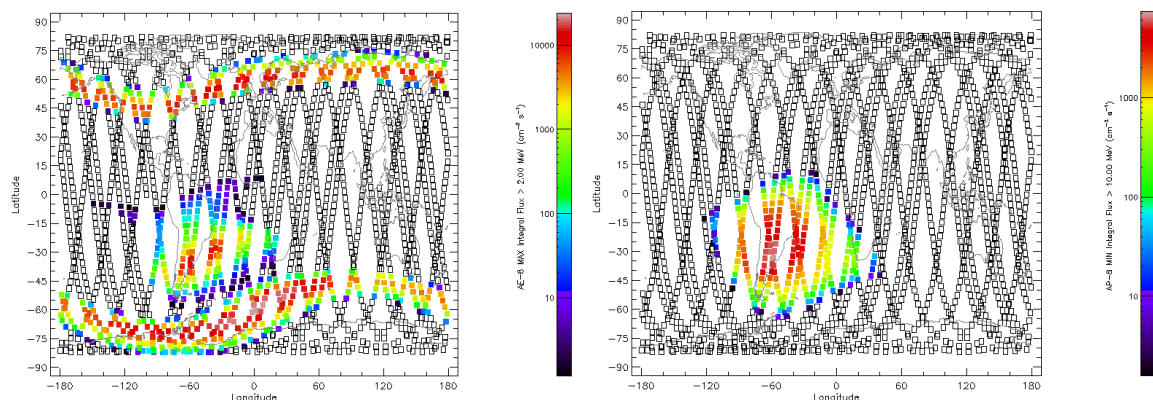

Figure 8: Integral flux maps for >2 MeV electrons (LHS) and >10 MeV protons (RHS) overlaid on a 800 km sun synchronous orbit trajectory.

Differential spectra from these calculations are shown in Figure 9. Also shown is a spectrum for solar energetic protons (SEPs) over the 10-year mission duration. As SEP occurrence is a probabilistic process, this spectrum is shown at the 90% confidence level (i.e. there is a 90% probability that the fluence will not be exceeded over this time frame).
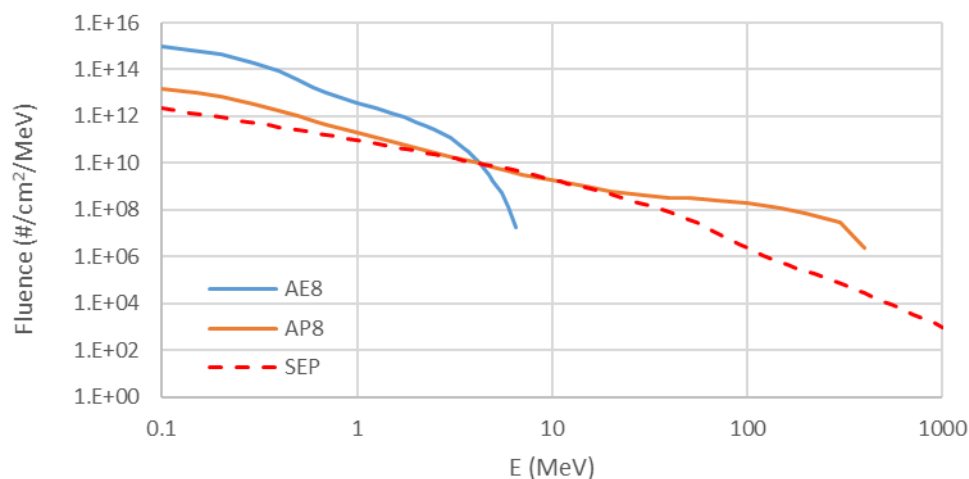
Figure 9: Differential electron and proton spectra for a 10 year period in 800 km sun synchronous orbit. Trapped spectra are shown for electron (AE8) and protons (AP8) and cumulative solar protons (SEP) calculated using the SAPPHIRE model are shown at the 90% confidence level.

Ionising dose as a function of shielding depth was calculated with SHIELDOSE-2 using the spectra shown in Figure 10. Planar shielding geometry was assumed as this is most suitable for locations that are relatively lightly shielded (at higher levels of shielding spherical geometry is more appropriate). It is clear from this plot that the influence of solar protons on dose is likely to be negligible for this environment – this is useful as it allows linear scaling of dose values for different mission durations.
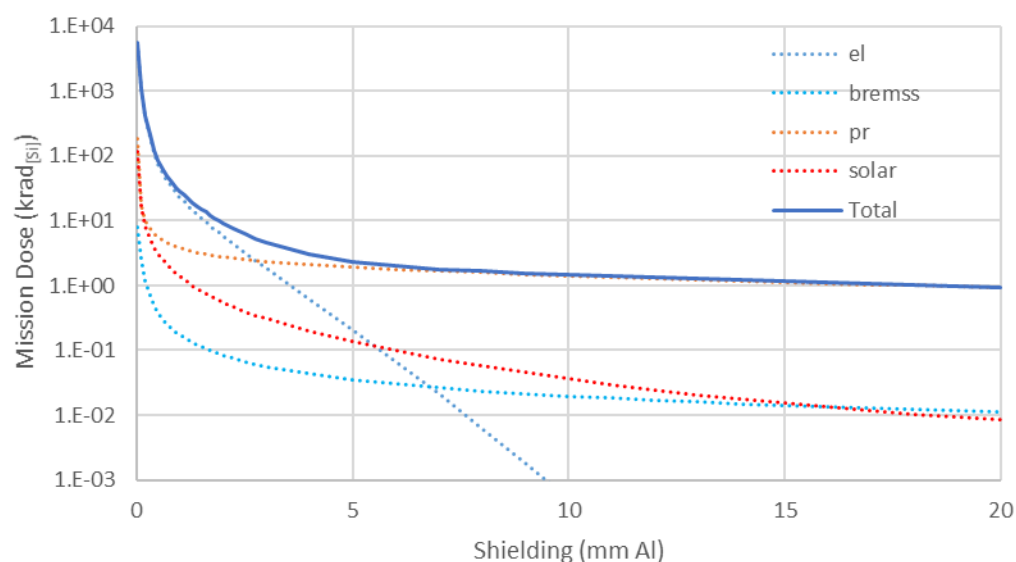

Figure 10: Ionising dose as a function of shielding depth (aluminium-equivalent) over the course of a 10 year LEO mission. A planar (slab) geometry is assumed. Contributing components ("el" = electron direct ionisation, "pr" = proton direct ionisation, "bremss" = Bremsstrahlung radiation and "solar" = SEPs at 90% confidence) are shown as dotted lines.

For example, these calculations predict a total ionising dose of ~3 kRad$_{[Si]}$ over the 10 year LEO mission if 4 mm Al-equivalent shielding were assumed. The figure for 1 mm of Al-equivalent shielding is an order of magnitude higher at ~30 kRad$_{[Si]}$, and the figure for 2mm of shielding is 9 kRad$_{[Si]}$. The assumed level of spacecraft shielding is critical in determining the appropriate dose to evaluate the performance of candidate components.

6.1.4.1.1   REEF Calculations

Monte Carlo particle transport calculations were used to simulate a simple planar geometry whereby a 100 micron silicon sensitive volume is shielded by a 100 micron layer of fused silica (SiO_2) packaging material. The source itself is encapsulated with a thin layer of stainless steel attenuating the raw strontium-90 beta spectrum before incidence on the device under test. Figure 11 shows the raw and attenuated spectra alongside the additional (albeit small) attenuation due to component packaging. The estimated dose rate for an incident current of 1 pA/cm^2 (corresponding to a source-sample separation of approximately 9 cm) is ~1 kRad$_{[Si]}$ per hour. This dose rate could potentially be increased substantially by reducing the source-to-sample separation, however, as the strontium is (approximately) a point source, too high a dose rate could potentially introduce uncertainty due to anisotropy of the irradiation. It has been calculated that the micron layer thickness of the processor packages only makes a minor difference to the total TID and should be considered a minor risk.
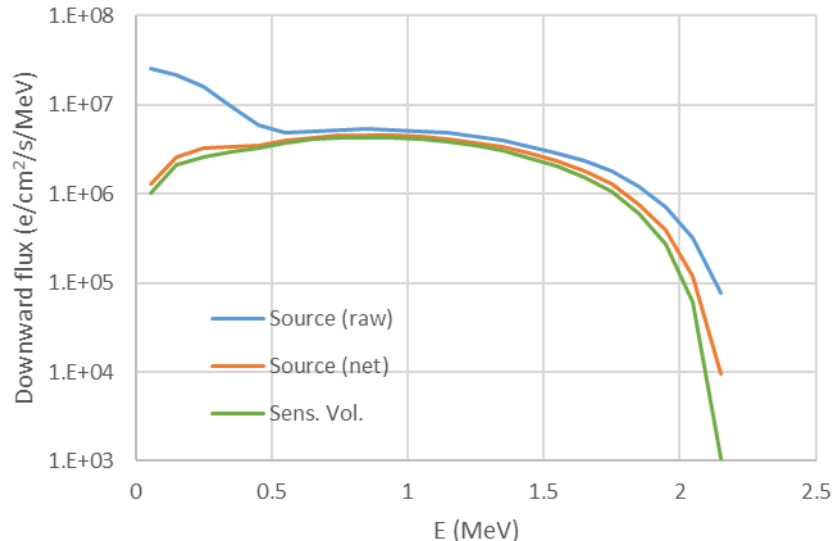

Figure 11: REEF electron spectra for the raw source (blue line), net source spectrum after encapsulation packing (orange line) and spectrum after nominal component shielding (green line). Although the impact of source encapsulation on the spectrum is clear, the impact of thin layers of component shielding is relatively small.

6.1.4.1.2   Summary

Standard radiation environment tools were used to calculate the total ionising dose for a 10 year mission in 800 km LEO. The dose has a strong dependency on assumed spacecraft shielding, for example ranging from ~3 kRad$_{[Si]}$ to ~30 kRad$_{[Si]}$ for 4 mm and 1 mm Al-equivalent shielding respectively. In parallel the dose rate in REEF at a particular reference point for incident electron current (~1 kRad$_{[Si]}$ per hour) was calculated Therefore, based upon the specification of 2mm shielding, the expected dose will be ~9 kRad$_{[Si]}$. The conclusion was that the total mission dose could be achieved in REEF in a timescale of hours to tens of hours of exposure. Significantly higher and lower dose rates are achievable; however these are unlikely to be necessary unless it is desirable to expose devices under test to doses far in excess of the expected mission dose.

6.1.5   Test Plan

Given the above test analysis, the team decided to test four targets to 10 kRad. This was considered the pass criteria for a 10 year, 800 km sun synchronous mission. Should time allow and the target survives this dose, the plan was to expose one of these four parts to as high a dose as was achievable before observing failures through the test rig utility.

6.2   SAMA5D3 Results

6.2.1   Overview

Boards Tested: 4/4

Batch Markings:

    A.   CU 1505 A A2GCVA

NOTE: Two of these boards were tested beyond 100 kRads. Although this was not intended through the original test plan, it was due to the test starting and running over a weekend.

Board	Batch	Test Time (hrs)	TID (krad)	Start Voltage (V)	End Voltage (V)	Start Current (mA)	End Current (mA)	NOTES
1	A	92.3	120.0	3.297	3297	99	101	No observed failures at end of test Dose rate = 1.3 krads/hr
2	A	96.8	125.9	3.304	3.304	101	102	No observed failures at end of test Dose rate = 1.3 krads/hr
3	A	43.8	57.0	3.296	3.297	101	102	No observed failures at end of test Dose rate = 1.3 krads/hr

4	A	19.7	25.7	3.293	3.293	129	135	No observed failures at end of test Dose rate = 1.3 krads/hr

6.2.2 Evidence Files

Board 1: SAMA5D3_DESTRUCTION.txt

Board 2: SAMA5D3_BOARD2.txt

Board 3: SAMA5D3_BOARD3.txt

Board 4: SAMA5D3_BOARD4.txt

These raw data files are available by request to the OSSAT team. We are happy to supply this information, but it needs to be supplemented with a format description.

6.2.3 Error Recovery Actioned

Board	Error Recovery Steps Actioned	Results
1	None	N/A
2	None	N/A
3	None	N/A
4	None	N/A

6.2.4 Current Consumption Observations

6.2.4.1 Shorter Duration Tests

Three of the SAMA5D3 boards had a similar current consumption of 99 – 101 mA. Unfortunately, due to the higher current channel requirement of the Digital Multi Meter (> 100 mA), finer measurements than 1 mA resolution were lost during the tests of the SAMA5D3. However, all four boards consumed more the specified 300mW specified in the evaluation criteria (see section 5). The paper analysis suggested a power consumption considerably lower than the actual value observed.

Note, because of the limited resolution, each of the following figures use a savgol filter to average out the data to make it readable. Figure 12 shows the power consumption during the USART test up to 57 kRads, it can be seen that the current doesn't increase apart from the first few kRads, most likely due to warm up. Figure 13 and Figure 14 are from board 4, which had a higher current consumption of 133 mA, showing RAM and USART tests respectively.
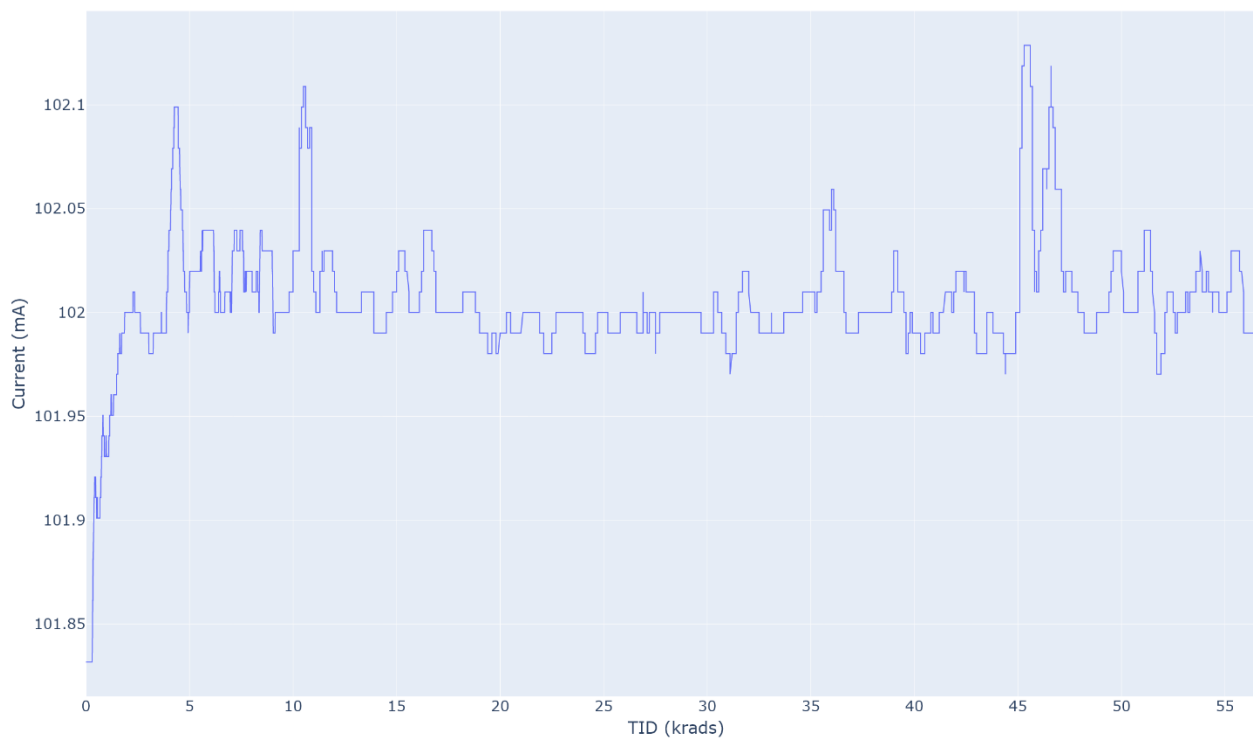
SAMA5D3 Board ID: 3 Test:USART

Figure 12: Current consumption of the USART test on SAMA5D3 Board 3, with TID of up to 57 krads.

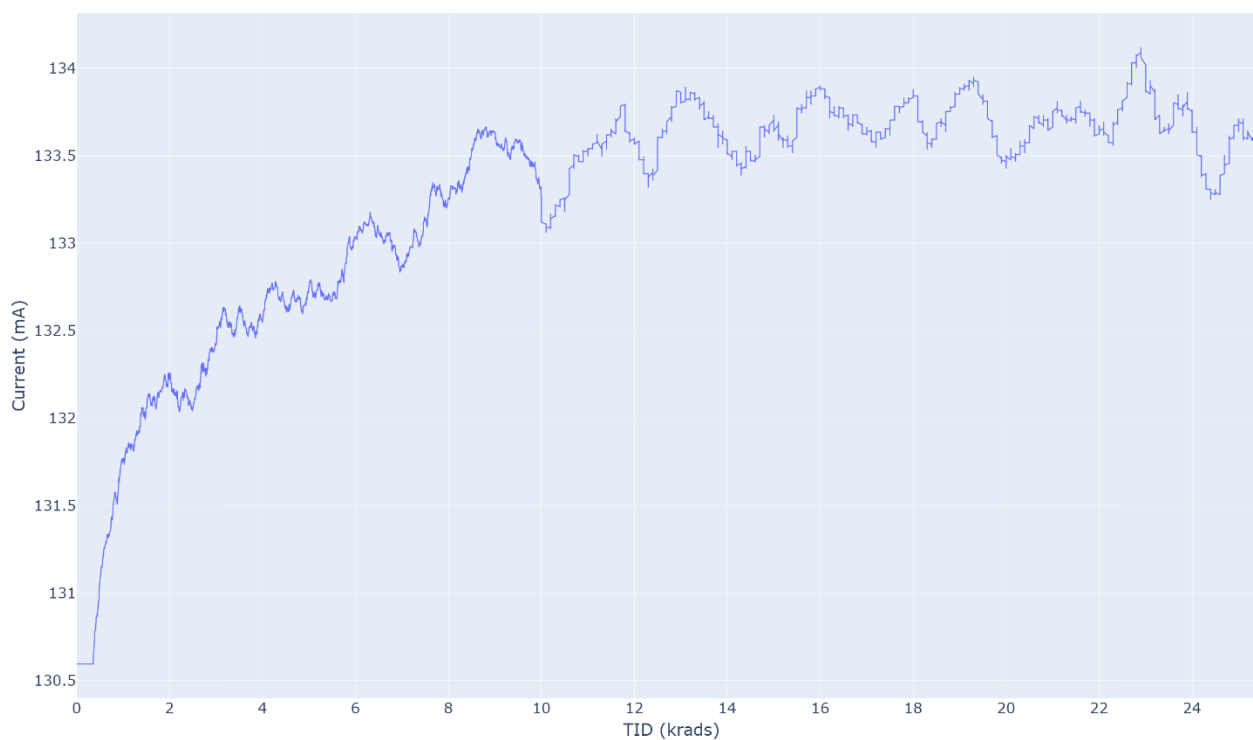SAMA5D3 Board ID: 4 Test:RAM Filtered

Figure 13: Current consumption of the RAM test on SAMA5D3 Board 3, with TID of up to 57 krads.
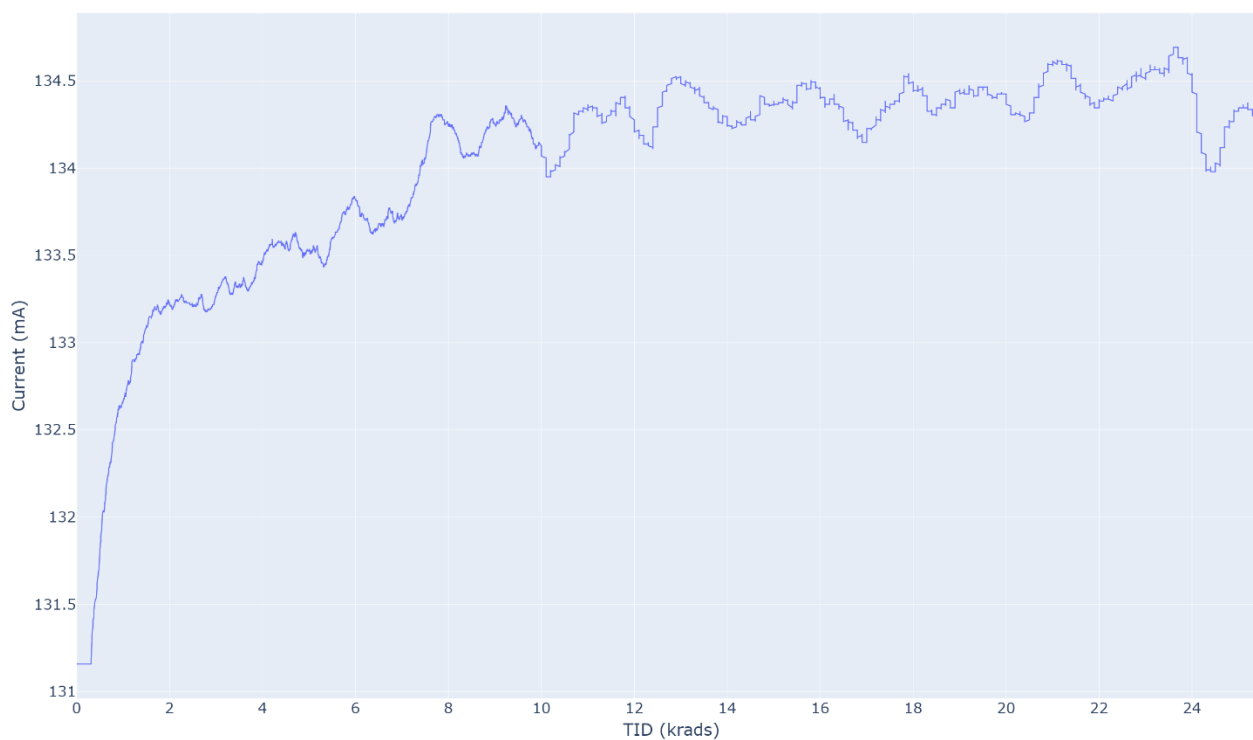
SAMA5D3 Board ID: 4 Test:USART

Figure 14: Current consumption of USART test on SAMA5D3 Board 4, with TID of up to 25 krads.

6.2.4.2   Destruction Test

For the SAMA5D3, two destruction tests were effectively carried out. This was because the first test showed little performance degradation, and no errors. To check this result the second board was irradiated over the weekend. Both of these boards reached 120 krads. The average current increase during these tests was 0.5 mA (see Figure 15 and Figure 16, after the initial warm up). The unfiltered data is shown in Figure 17.
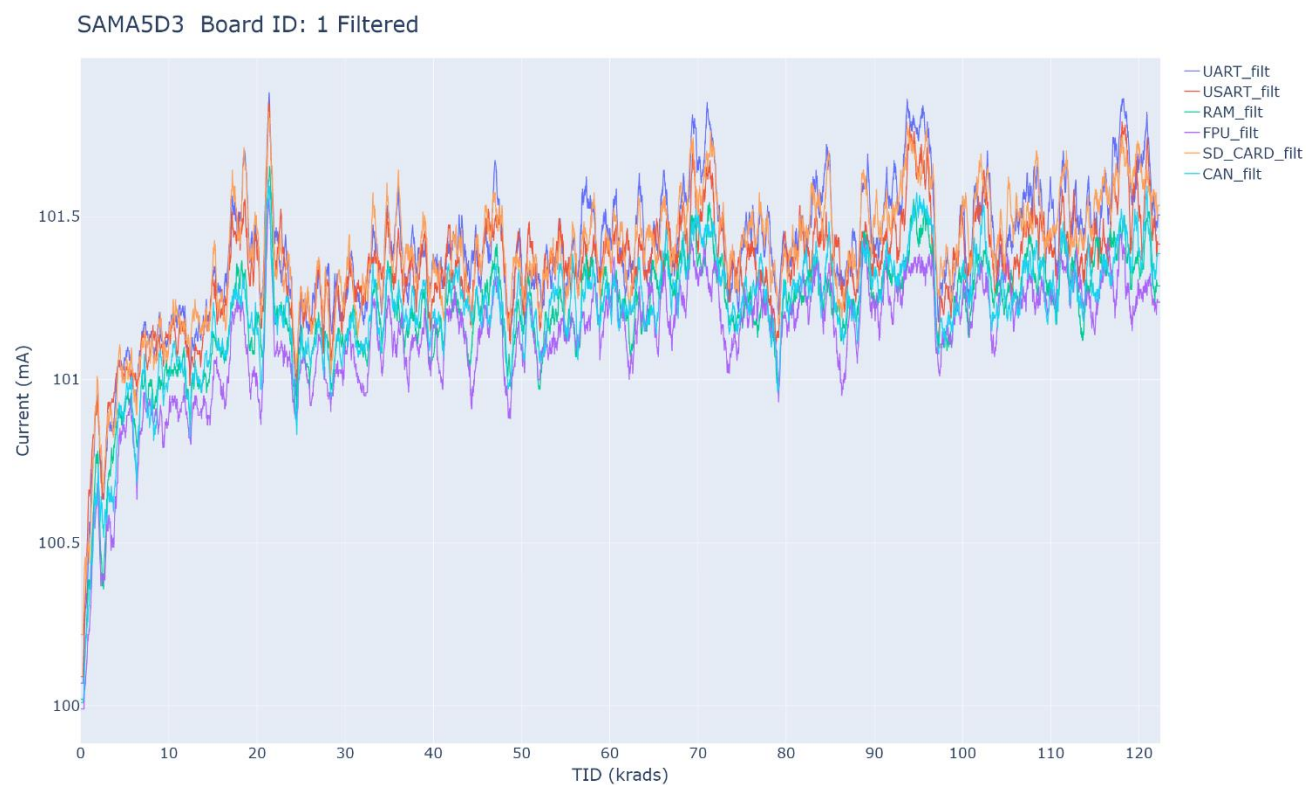
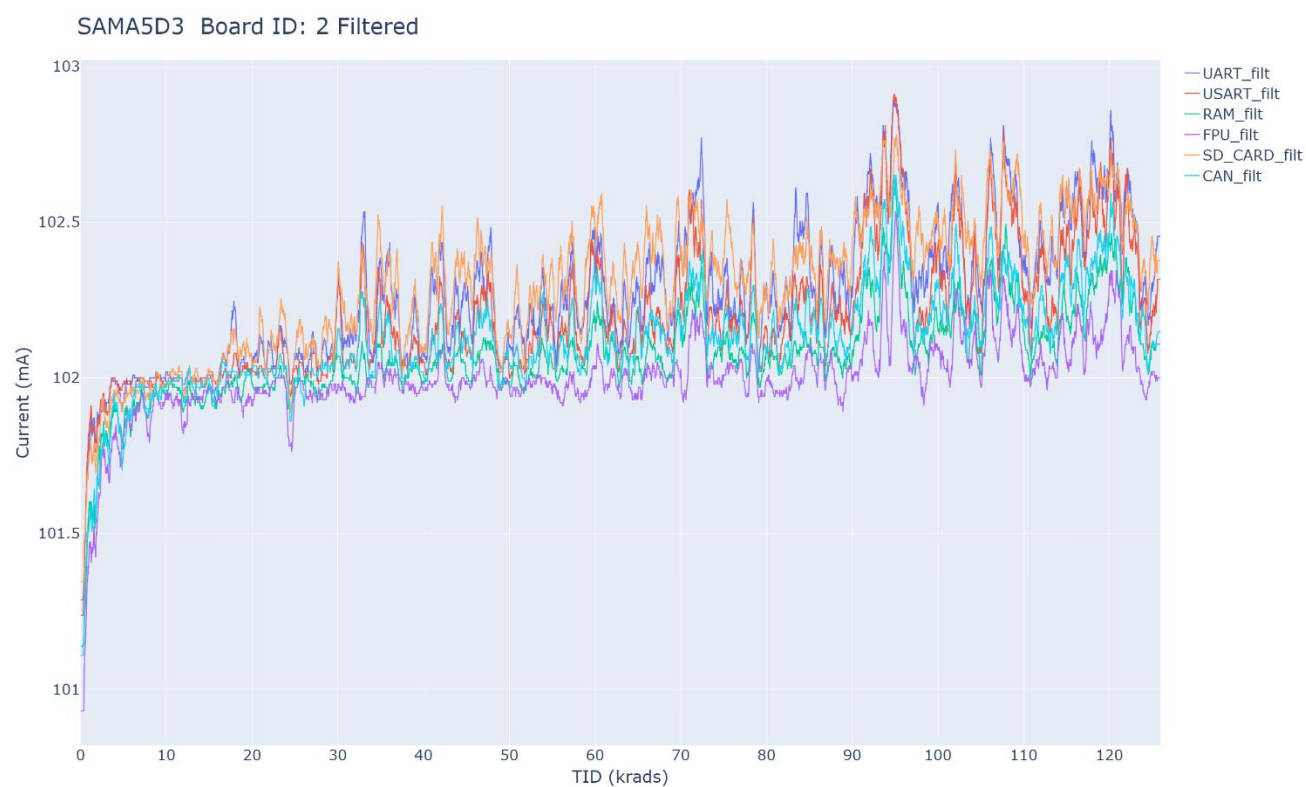*Figure 15: Current consumption of all tests on SAMA5D3 Board 1 - first destruction test*

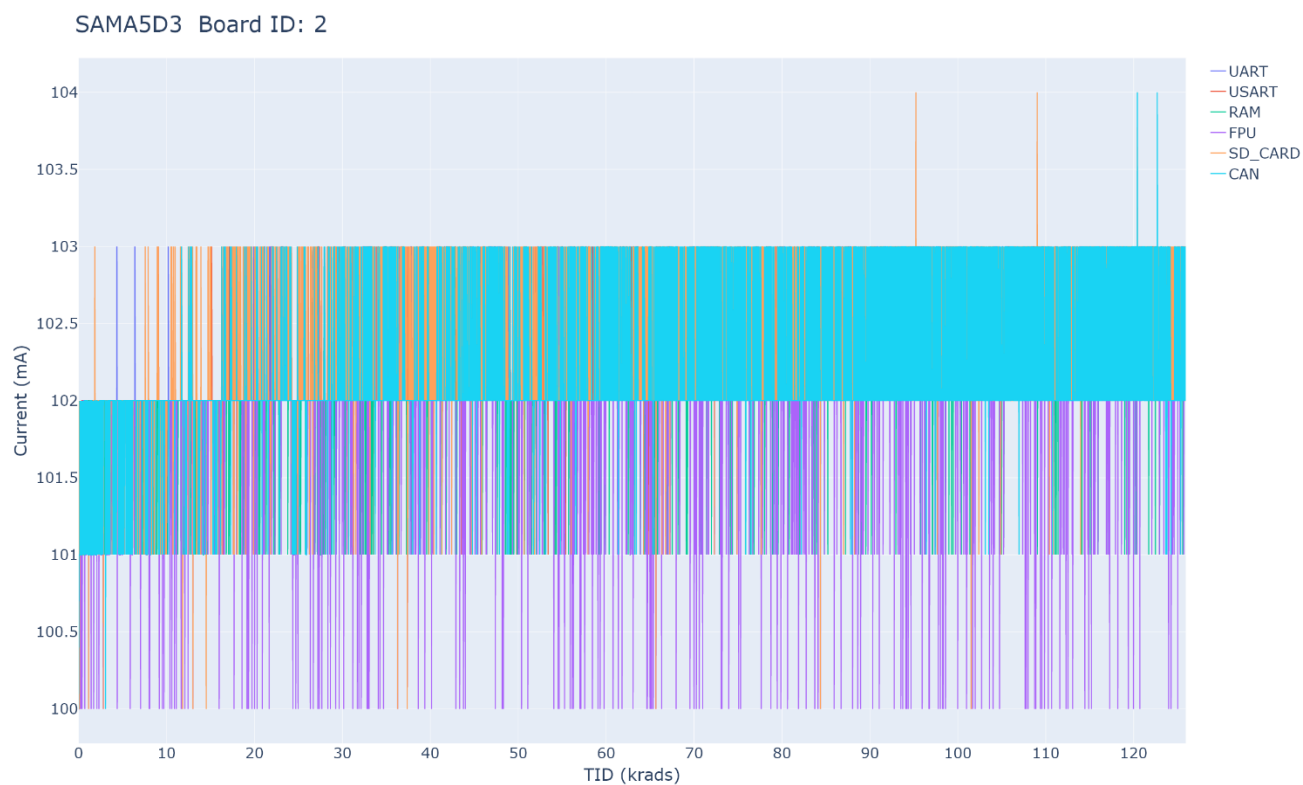*Figure 16: Current consumption of all tests on SAMA5D3 Board 2 - second destruction test*

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Figure 17: Unfiltered data of Figure 16.

6.3 Processor Performance

6.3.1 Test Setup

The OSSAT team is aware that major performance issues occur in relation to writes to a file system. Therefore, in order to assess performance, software was integrated as shown in Figure 18.
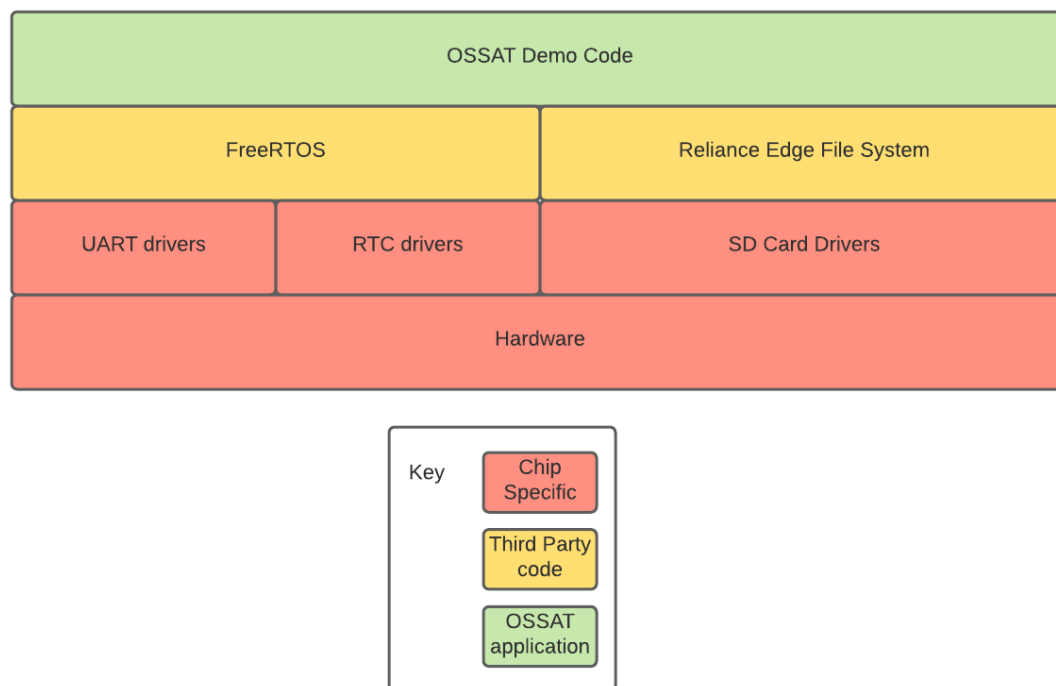
Figure 18: OSSAT SAMV71 file system performance

FreeRTOS was selected because of its strong, open source community, small memory footprint and general simplicity.

The Reliance Edge File System was selected because it is open source and is designed to work reliably following sudden power loss during a commit.

A worst case scenario for platform software file writes was estimated. This resulted in a worst case burst requirement of 6800 bytes across 12 different files in 50ms.

Tests were performed without the processor's cache enabled, this is because the SAMA5D3 does not have ECC memory protection on its cache memory. The feature size of cache means that it is often the weakest part of the chip with respect to single event upset and is therefore disabled.

6.3.2 Test Results

Tests were run 10 times, writing data to 12 files from 12 different FreeRTOS tasks. This involved the file write and a "red_transact()". This "red_transact()" commits the change to the underlying media (an SD card was chosen). Therefore, the burst requirement of 50ms applies to the file write time only. See section 7 for conclusions.

6.3.2.1 *Release build with cache disabled*

File write max time: 35.2ms

File write average time: 33.56ms

File write std dev: 3ms

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red_transact() max time: 87ms

7 Conclusions

Following the initial testing performed on the SAMA5D3, it remains a candidate OSSAT processor, both from a performance and radiation tolerance perspective. Follow on work is needed to validate this further. However, we did find that developing "bare metal" software for this processor was not an easy task. The toolsets are setup around a Linux (Yokto) O/S including a U-Boot loader. The processor is also not as feature rich as the other two processors (the Atmel/Microchip SAMV71 and the ST Microelectronics STM32H753) that we evaluated. Despite the fact that this processor seemed very resilient wrt TID radiation, the OSSAT team found the other two processors much easier to configure and use.

It is capable of writing to files at a speed which is fast enough for the needs of the OSSAT platform requirements (with cache disabled consuming approximately. 70% of the processor's processing run time under worst case burst write conditions).

It is also capable of withstanding significant TID without failure. Through analysis, a 10 year 800km sun synchronous orbit would equate to approximately 10 kRads of radiation dose. None of the samples tested failed in any detectable way, two of these were tested to 120 kRads.

8 Future Work

Further work is required in order to derisk the SAMA5D3 as a suitable processor for the OSSAT platform. The OSSAT team are therefore planning the following:

8.1 SEU/Latch-up testing

The OSSAT team have a test plan drafted for a proton irradiation test campaign to test for tolerance against the Single Event Upset and Latch up effects.

8.2 Further performance testing

The design goal is to develop an AOCS system capable of running AOCS loops at up to 12Hz. This would be a major performance requirement on the SAMA5D3 processor. Therefore, a further task would be to develop representative AOCS software that would exercise the processor and assess its suitability to this task.

9 Credits

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