OPEN SOURCE SATELLITE

SAMV71 Radiation Test Report

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Table of Contents

Table of Figures 2
1 Document History 1
2 References 1
3 Introduction 2
4 Scope 2
5 Processor Selection 2
5.1 Selection Criteria 2
5.1.1 Performance Requirement 3
5.1.2 Power Consumption Requirement 3
5.1.3 Floating Point Operations Requirement 3
5.1.4 Program Memory Requirement 4
5.1.5 Data Memory Requirement 4
5.1.6 Mass Memory Requirement 4
5.1.7 Thermal Requirement 5
5.2 Qualitative Criteria 5
5.2.1 External Memory Interfaces 5
5.2.2 Existing Radiation Tolerance data 5
5.2.3 Existing SEU Protection 5
5.2.4 Development Tool Compatibility 5
5.2.5 RTOS availability 5
5.2.6 Field-Programmable Gate Array (FPGA) configurability 6
5.2.7 Cyclic Redundancy Check (CRC) Generation 6
5.2.8 Encryption/Decryption AES256 6
5.2.9 Authentication (e.g. SHA-1) 6
5.2.10 Flight Heritage 6
5.2.11 Obsolescence 6
5.2.12 Interfacing 6
5.3 SAMV71 Specification (Part #ATSAMV71Q21) 6
5.4 Evaluation Summary 9
6 SAMV71 test results 9
6.1 Total Ionising Dose Radiation Test 10

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6.1.1 Test Setup 10
6.1.2 The Target Under Test 11
6.1.3 Test Rig Setup 14
6.1.4 Test Analysis 16
6.1.5 Test Plan 20
6.2 SAMV71 Results 20
6.2.1 Overview 20
6.2.2 Evidence Files 21
6.2.3 Error Recovery Actioned 21
6.2.4 Observed Failures/Recoveries 22
6.2.5 Annealing Post Destruction Results 23
6.2.6 Current Consumption Observations 23
6.2.7 Destruction Test 25
6.3 Processor Performance 26
6.3.1 Test Setup 26
6.3.2 Test Results 27
7 Conclusions 28
8 Future Work 28
8.1 SEU/Latch-up testing 28
8.2 Further performance testing 28
9 Credits 28
10 Appendix A 29

Table of Figures

Figure 1: REEF equipment at the University of Surrey 10
Figure 2: SAMV71 Xplained Eval board. Image Credit: Microchip 11
Figure 3: SAMV71 behind an aluminium shield 11
Figure 4: SAMV71 inside REEF 12
Figure 5: SAMV71 in test software loop 13
Figure 6: REEF Test rig setup 14
Figure 7: REEF Test Rig Utility GUI. 15
Figure 8: Automatic recovery from ADC errors 16
Figure 9: Integral flux maps for >2 MeV electrons (LHS) and >10 MeV protons (RHS) overlaid on a 800 km sun synchronous orbit trajectory. 17

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Figure 10: Differential electron and proton spectra for a 10 year period in 800 km sun synchronous orbit. Trapped spectra are shown for electron (AE8) and protons (AP8) and cumulative solar protons (SEP) calculated using the SAPPHIRE model are shown at the 90% confidence level.....18
Figure 11: Ionising dose as a function of shielding depth (aluminium-equivalent) over the course of a 10 year LEO mission. A planar (slab) geometry is assumed. Contributing components ("el" = electron direct ionisation, "pr" = proton direct ionisation, "bremss" = Bremsstrahlung radiation and "solar" = SEPs at 90% confidence) are shown as dotted lines.....18
Figure 12: REEF electron spectra for the raw source (blue line), net source spectrum after encapsulation packing (orange line) and spectrum after nominal component shielding (green line). Although the impact of source encapsulation on the spectrum is clear, the impact of thin layers of component shielding is relatively small. 19
Figure 13: SAMV71 current consumption by the RAM test up to 10 kRads TID 23
Figure 14: Comparison of current consumption of each of the different memory tests up to 10 kRads on the SAM71. The ECC, AES and the SD-CARD all have identical current consumption, hence only the AES is visible on this plot. 24
Figure 15: Comparison of current consumption of each of the different interface tests up to 10 kRads on the SAM71. The UART and USART draw the most current, CAN the least. After a TID of 10 kRads, the processor was drawing 0.3 mA more current when running each interface test.....24
Figure 16: Comparison of current consumption of each of the different timer tests up to 10 kRads on the SAM71 25
Figure 17: Current consumption for SAMV71 destruction run, for the USART tests. Note: The green vertical lines indicate gaps in the data, due to testrig failures. 26
Figure 18: OSSAT SAMV71 file system performance 27
Figure 19: Cortex M7 ECC features.....29

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1 Document History

Please see the following record of revisions:

Document Revision	Document Status	Change Description
01	RELEASED	Initial revision post internal review.

2 References

The following references are applicable to this document.

Document Reference	Document Title	Date	Reference in this Document
44003E	ATARM-SAM V71-Datasheet	12th Oct 2016	[SAMV71 Datatsheet]

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3 Introduction

One of the key components of the Open Source Satellite (OSSAT) command and data handling system is the microprocessor for the On Board Computer (OBC). Microprocessors that have been designed to be radiation-hardened for the harsh space environment are expensive and tend to have poor performance compared to Commercial-Off-The-Shelf (COTS) equivalents that leverage the latest innovations in microprocessor technology. The OSSAT team possesses decades of experience in using COTS components in Low Earth Orbit (LEO) and intends to leverage the capabilities of the latest terrestrial technology in the development of the OSSAT platform computer.

The OSSAT team performed a research and development project to further the understanding of COTS processors, in partnership with the Surrey Space Centre (SSC) at the University of Surrey, UK, with support from Research England's SPRINT programme[1]. The OSSAT-SSC project team evaluated the latest available COTS microprocessors[2] and assessed their suitability in terms of performance with a view to test their resilience to the harsh space radiation environment. Three COTS processors were downselected and subjected to a series of research tests to determine processor performance and space environmental resilience.

4 Scope

This document is the first in a set of three reports that presents the results of the microprocessor research. Each document describes:

- The justified evaluation criteria for the selected processors.
- The key features of each processor.
- The results of the two types of tests performed on each processor:
    - A test of the processor's performance.
    - A test of the processor's susceptibility to the effects of the space radiation environment.

This first document gives the results of this research in relation to the first of the three downselected processors, the Atmel/Microchip SAMV71.

5 Processor Selection

5.1 Selection Criteria

Several quantitative and qualitative criteria were defined in order to evaluate a suitable microprocessor to integrate into the OSSAT platform. This section presents the criteria with justifications listed in descending order of importance.

[1] https://sprint.ac.uk/about-us/

[2] https://www.sprint.ac.uk/news-stories/kispe-space-joins-sprint-to-source-microprocessors-for-next-generation-microsatellite-platforms/

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5.1.1 Performance Requirement

The **minimum** performance figure of **200 DMIPS** has been defined.

5.1.1.1 Performance Requirement Rationale

The OSSAT team has experience in working with OBCs for a wide range of different missions. We are aware of the increasingly demanding performance requirements that flight software places on OBCs for new and emerging mission needs. For example: higher (Attitude and Orbit Control System) AOCS algorithm execution rates (in the range of 4-12Hz to support increased agility), higher telemetry sampling rates (in the range of 20Hz to improve the speed of anomaly diagnosis) and larger files (log data will be plaintext in order to reduce the time required to interpret the data).

Our survey of commercially-available space OBCs identified products that have a performance of 50 to 60 DMIPS, which do not satisfy the performance criteria required to enable a new generation of space-enabled missions, applications and services. The 200 DMIPS represents a substantial improvement in this performance without a significant increase in power consumption.

The availability of a very high-performance platform processor can lead to a blurring of the boundary between platform and payload because of the temptation to embed payload operations within such a processor, potentially leading to complicated and blurred functionality. Our design philosophy is to maintain a platform-payload separation to eliminate the risk of mission-specific payload requirements driving changes and NRE on the platform design.

NOTE: The DMIPS measure takes no account of floating-point operations.

NOTE: Manufacturers often measure performance in units of either Coremarks or DMIPS. We adopted DMIPS because it seemed the most common measure. Where manufacturers gave measurements in Coremarks, we translated the figures approximately into DMIPS.

5.1.2 Power Consumption Requirement

The maximum amount of power consumed by the processor must **not exceed 300mW** at ambient temperature.

5.1.2.1 Power Consumption Requirement Rationale

Power consumption is always a principal consideration on space missions. The platform must consume as little power as possible in order to maximise the power available for payloads and thereby enhance mission utility. The OSSAT team intends to capitalise on advances in low power processing technology to identify potential options that satisfy this requirement. It is also important to recognise that, when conducting a paper exercise, power consumption figures quoted by manufacturers can be difficult to interpret. A pragmatic and appropriate level of effort was applied to ensuring that the comparison of power figures is fair.

5.1.3 Floating Point Operations Requirement

The processor must be capable of processing arithmetic on **floating point numbers**.

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5.1.3.1 Floating Point Requirement Rationale

The platform processor will need to perform AOCS algorithms at relatively high speeds (more than 4 Hz and up to 12Hz). To code these algorithms in integer maths is not practical. The processor therefore needs to support floating point operations. NOTE: this can be achieved either through the integration of a floating-point unit or otherwise through a compiler that can translate from floating point to integer maths and subsequently compile. In this case, the general performance figure should be increased. As a preference, the processor would have a floating point unit (single or double precision).

5.1.4 Program Memory Requirement

The processor must be able to address at least **50MB** of **program memory** (the non-volatile memory used to hold the program).

5.1.4.1 Program Memory Requirement Rationale

Programs are anticipated to be in the region of 100's of kilobytes rather than 50MB. For example, KISPE recently integrated FreeRTOS with a Board Support Package (BSP) and a number of tasks all compiled down to <200kB of Program data on an ARM Cortex-M7. However, other Linux-based operating systems, that potential OSSAT users may wish to implement, have a much bigger footprint. Also, the introduction of run time uploadable tasks may result in far less efficient use of program memory. 50MB provides capacity to accommodate a wide range of programs. NOTE: This memory can be on-chip or off chip (with a preference for on chip so long as it has Error Correcting Code (ECC) protection).

5.1.5 Data Memory Requirement

The processor must be able to address at least **64MB** of **data memory** (the volatile memory used by the program during execution).

5.1.5.1 Data Memory Requirement Rationale

There are a number of consumers of data memory, including:

- Buffering data destined for the file system, depending upon file system performance, this may be significant.
- Buffer I/O
- Data structures for the RTOS

The OSSAT team have recently integrated FreeRTOS with a BSP and a number of tasks, all compiled down to use <400kB of data memory that was statically allocated). The amount of required memory may vary greatly and therefore 64MB was defined to address anticipated needs.

NOTE: This memory can be on-chip or off chip. Ideally, this memory would be on chip and with ECC protection.

5.1.6 Mass Memory Requirement

The processor must be able to accommodate at least **4GB** of **mass memory** to house the file system.

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5.1.6.1 Mass Memory Requirement Rationale

Platform telemetry data will be stored alongside operational timetables that schedule activities and configuration files. This data will be stored in a file system that is housed on a mass memory. The mass memory should ideally be non-volatile so long as the file integrity can be maintained in environments susceptible to Single Event Upsets (SEUs). Some non-volatile memory needs to be baselined since the spacecraft configuration will be stored in a memory that needs to survive power interruptions and resets.

5.1.7 Thermal Requirement

The processor must be able to fully operate between -40 to +85 degrees C.

5.1.7.1 Thermal Requirement Rationale

This temperature range covers the majority of operating temperatures that will be experienced by the spacecraft. It is also the typical range for the majority of automotive electronic components that are being considered for OSSAT, giving the maximum flexibility to the thermal design of the spacecraft.

5.2 Qualitative Criteria

A number of other features and properties are relevant to the platform processor selection, including:

5.2.1 External Memory Interfaces

SEU memory protection can be implemented off-chip in hardware if the chip supports external memory interfaces.

5.2.2 Existing Radiation Tolerance data

Any existing data about the radiation tolerance of the processor would be beneficial. Furthermore, some parts have pin compatible radiation tolerant equivalents. These parts are potentially more relevant because the radiation tolerant equivalent part could be used for “beyond LEO” missions without needing to re-engineer these core elements of the platform software or PCB layout.

5.2.3 Existing SEU Protection

As the feature size of components has reduced, commercial processors have become susceptible to SEUs even when used in terrestrial applications. Therefore, some vendors have introduced error detection or error detection and correction technology into the silicon. Availability of SEU mitigation, such as single bit per word error detection and correction, is an important consideration.

5.2.4 Development Tool Compatibility

The availability of tools to aid the development of software for the processor and to model power consumption was considered, as was whether the tools are open source, whether support is available for a fee, and how large the userbase is.

5.2.5 RTOS availability

The quantity of Real Time Operating Systems (RTOS’s) that support the processor was assessed, as was whether the RTOS’s are open source.

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5.2.6 Field-Programmable Gate Array (FPGA) configurability

FPGAs offer an extra degree of reconfigurability. FPGAs with embedded processors were therefore preferred and any FPGA hardware noted during the selection.

5.2.7 Cyclic Redundancy Check (CRC) Generation

Existence of hardware acceleration of CRC generation was evaluated because CRC generation will be a common task of the platform processor. It should be noted that the use of CRC protection should be weighed up against error detection and correction for communications interfaces.

5.2.8 Encryption/Decryption AES256

Existence of hardware acceleration to aid cipher/decipher was evaluated in order to satisfy the requirement for encryption to AES256: NOTE: the adoption of encryption must be weighed against power consumption, message sizes and the resulting effect on bit error rate.

5.2.9 Authentication (e.g. SHA-1)

Whether or not the processor includes hardware acceleration that aids authentication was assessed. This was considered because communications with the ground will need to be authenticated.

5.2.10 Flight Heritage

Previous in-orbit data, and information on the type of mission, if available, was evaluated.

5.2.11 Obsolescence

Production runs of components can be very short. This largely depends upon the industry for which the processor is manufactured. Chips manufactured for the automotive and aerospace industries are attractive because of the very long production runs, allowing the same components to be used across a series of different missions without needing to redesign the system.

5.2.12 Interfacing

The types and quantities of I/O interfaces that are supported by the chip was considered. Should specific technologies not be supported by the chip, supplementary devices could be used to provide the required interface.

5.3 SAMV71 Specification (Part #ATSAMV71Q21)

This is a high-end single core micro-controller, manufactured by Microchip Technology Inc. It has a low power ARM Cortex M7 32-bit core and many peripherals (see [SAMV71 Datatsheet]). It is a very popular and versatile chip that is designed for the automotive industry and costs approximately $15. This chip is particularly attractive because a radiation tolerant equivalent is also available from Microchip at around $4,000 per chip. Therefore, the commercial part could be used for LEO orbits and the Rad tolerant variant for harsh environments with minimal changes to the software and PCB layout.

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NOTE: The SAMV71 can only satisfy the mass memory requirement by using I/O outside of the memory controllers to address enough memory or by incorporating SD memory/MMC memory.

The outcome of the evaluation of the chip against the quantitative criteria is as follows:

Criteria	Target	Actual	Supplementary Circuitry required
Performance	200 DMIPS	640 DMIPS[3]	N/A
Power Consumption	300mW	250mW during radiation test	N/A
Floating Point	FPU desirable	Double Precision FPU	N/A
Program Memory	50MB	2MB (internal)	External program memory[4]
Data Memory	64MB	384kB (internal)	External data memory
Mass Memory	64GB	None (other than the data memory already mentioned)	SD/MMC interface to memory and up to 256MB SDRAM and 64 MB Static memory. SPI/I2C busses can be used as a further memory interface. The capacity of these memories is increasing all the time, a single chip can now hold up to 8GB. NOTE: SD/MMC memory can be used but this has very high memory densities that presents a risk (small transistor sizes are susceptible to SEU, and memory could be slow).
Thermal	-40 to +100 degrees C	-40 to +105 degrees C	N/A

The outcome of the chip against the qualitative criteria is as follows:

[3] This assumes the cache memory (which is ECC protected) is enabled.

[4] The processor can run code from external memory also. See https://www.avrfreaks.net/forum/compiling-program-ram-sam-v71-xplained-pro-card

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Criteria	SAMV71 capability
External memory interfaces	The chip has many interfaces but a maximum SDRAM size of 256MB is addressable and a maximum static memory size of 64MB is addressable. SD/MMC card interfaces are also available and SPI/I2C memories. It would be desirable for the chip to be able to address more SDRAM; the consequence of this is that it will lead to a slightly more complex design where more memory interfaces are used to achieve the required memory capacity. Furthermore, the additional memory interfaces are slower than internal memories.
Existing radiation tolerance data	A pin compatible radiation-tolerant chip is available from Microchip (part #ATSAMV71RT). Quoted rad tolerance for this part is *No Single Event Latch-up Below an LET Threshold of 60 MeV.cm2/mg @125°C, Total Ionizing Dose of 30 kRad (Si) RHA*. CERN have performed some SEU tests on the COTS part but the tests did not seem representative of the environment for OSSAT missions.
Existing SEU protection	The chip incorporates instruction and data cache, all of which is ECC protected. The protection on the cache is described in Appendix A. The chip also contains an enhanced embedded flash controller that interfaces to the internal chip flash. This contains an ECC capable of detecting 2 errors and correcting 1 unique error in 128 bits. External memory interfaces do not include any protection against SEU's which leads to the selection of memories that include their own ECC or the inclusion of extra circuitry between the processor and its memory to perform this function.
Development tools	There is a rich selection of development tools, both open source (e.g. Atmel Studio with GNU) and commercial (e.g. Keil C/C++ compilers). The chip is not suited to Linux-based operating systems due to the limited memory. The tools have a very wide user base (particularly Atmel Studio and GNU toolchain). Free support is available through a strong support forum. Commercial support is also available for commercial toolchains (IAR/Keil). There appeared to be no power modelling tools available for this chip.

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Criteria	SAMV71 capability
RTOS availability	The Open Source FreeRTOS is a popular, open source choice for this and other ARM based microprocessors. Existing compatible BSPs exist for a great many RTOSs.
FPGA configurability	This chip is not included within an FPGA; however an external FPGA could be incorporated in the platform computer design.
CRC Generation	There are CRC generation hardware accelerations as part of some IO peripherals (e.g. CAN bus) but there is no general-purpose acceleration. General purpose CRC acceleration would be helpful in order to support communications and other functions.
Encryption/Decryption	The SAMV71 has dedicated hardware for AES256, 192 and 128 algorithms that accelerate common cipher/decipher.
Authentication	The chip has hardware acceleration for SHA-1, SHA224 and SHA256
Flight Heritage	No information has been found about this specific chip being used in space applications previously.
Obsolescence	The part is a popular choice within the automotive industry and is therefore a good choice in terms of the length of production runs.
Interfaces	1 * Ethernet 1 * USB 2.0 ITU-R BT image sensor interface 2 * CAN-FD 3 * USART 5 * UART 3 * I2C 2 * SPI 1 * Quad SPI 1 * I2S 1 * SDIO/SD card/MMC, 4 * 3 channel timer/counters/PWM 1 * 2 channel DAC 2 * 16-bit ADC (24 channels total)

5.4 Evaluation Summary

The SAMV71 matches the defined evaluation criteria well from the perspective of power consumption, run-time processor power and floating point support but lacks the required memory. Therefore, it would need some supplementary external memory.

6 SAMV71 test results

Following the down-selection of this chip, the following tests were performed using evaluation hardware.

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6.1 Total Ionising Dose Radiation Test

6.1.1 Test Setup

6.1.1.1 Test Facility

The Realistic Electron Environment Facility (REEF), located at the University of Surrey, UK, and operated by research colleagues from SSC exposes samples in vacuum to a ~2.5 GBq Sr-90 source. Strontium-90 provides an excellent practical option for the provision of long-duration, low-intensity exposures as it allows uninterrupted irradiations over the required long periods with an electron spectrum that is appropriately representative of the real space environment.

Figure 1: REEF equipment at the University of Surrey

The REEF can be used to test materials and components for their vulnerability to both internal charging and total ionising dose phenomena. The dose rate is proportional to electron current and thus is primarily determined by the source-to-sample separation distance in the experimental setup. Changes to the electron spectrum due change due to component shielding. This was taken into account (see section 6.1.4.1).

The dynamic range of normal incident electron current achievable with REEF is wide, ranging from ~6 pA/cm^2 at low (~3.5 cm) source-sample separation to ~0.3 pA/cm^2 at high source-sample separation (~16 cm). Higher currents can in theory be achieved at even smaller separations, though this would be at the expense of the assumption of normal incidence irradiation. Further reductions in current are achieved by adding planar aluminium shielding in between the source and sample.

The processor components to undergo testing were exposed to radiation equivalent to a 10 year, 800km, sun synchronous LEO mission. Upon completion of the REEF test for each board, any boards that showed forms of damage were

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tested again outside REEF to test for any potential annealing effects following irradiation.

6.1.2 The Target Under Test

In order to generate statistically relevant information, four SAMV71 Xplained evaluation boards featuring the downselected chip (the “Target”) were irradiated.

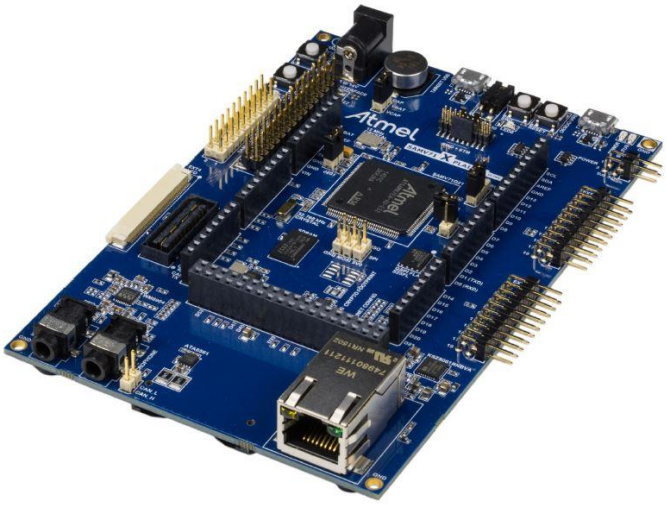

Figure 2: SAMV71 Xplained Eval board. Image Credit: Microchip

The intent of the test was to assess the radiation tolerance of the processor only, therefore the rest of the components were shielded from the radiation source as shown in Figure 3.

Figure 3: SAMV71 behind an aluminium shield

Each evaluation board was placed inside REEF and the radiation source positioned in order to test at a 1 kRad/hr dose rate as shown in Figure 4.

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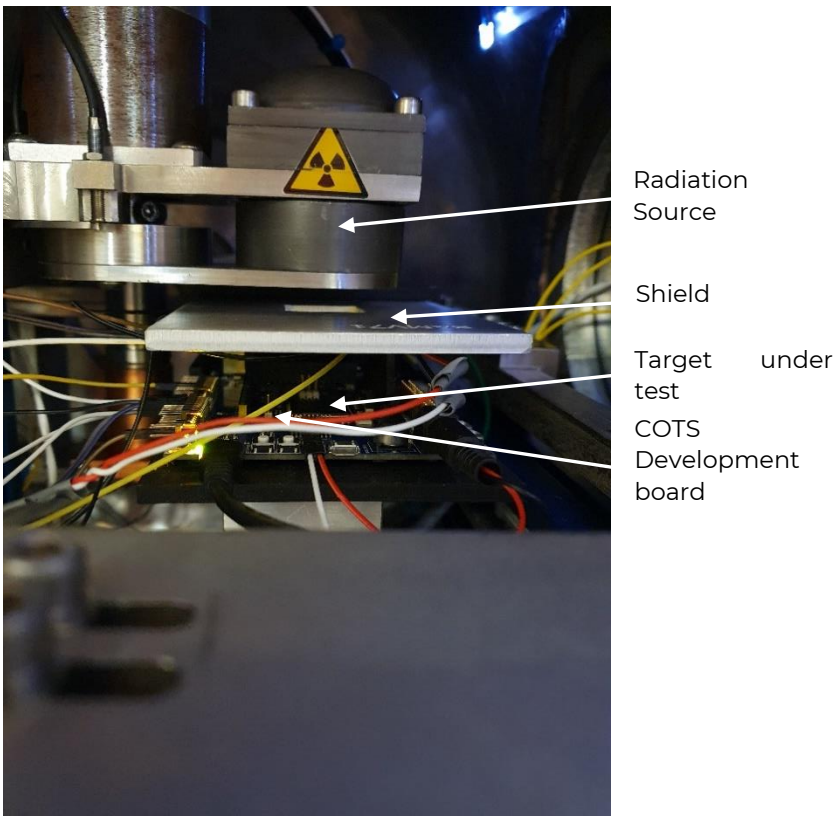

Figure 4: SAMV71 inside REEF

6.1.2.1 Target Software

The target processor was powered during irradiation. It ran software exercising various I/O interfaces and memories. The Test cycle repeated autonomously as illustrated in Figure 5 (NOTE: the wait between tests was reduced to 3 seconds in contrast to this figure. The original rationale for 30 seconds related to the anticipated time required to ensure a current & voltage measurement during the test. However, the current and voltage measurement mechanism proved faster than anticipated).

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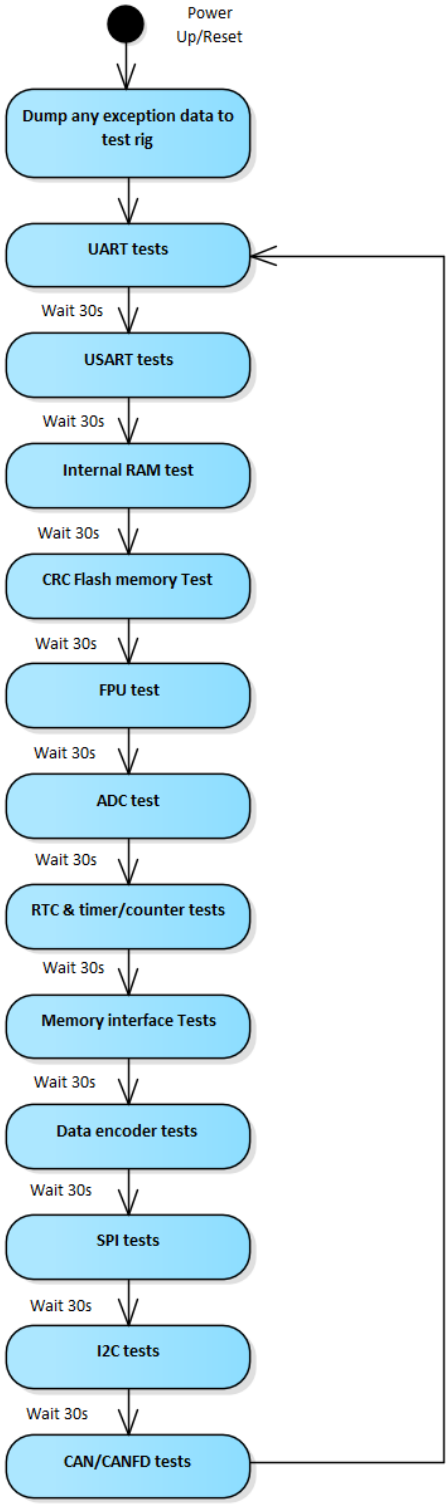

Figure 5: SAMV71 in test software loop

The tests were as follows:

- The I/O test for UART, USART, SPI and I2C included signalling at the physical layer which were looped back so that both transmission and reception were tested.

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- ADC values were read through from known analogue values into the software through the ADC hardware.
- The data encoding test included a test of known data input and output to and from the crypto hardware peripheral.
- The on chip RAM was tested using a scrub, read, write method.
- The internal Flash memory executed the code to perform all of these tests, a CRC of the Flash image was stored to an SD card and the Flash memory CRC was calculated once per test loop and compared to the value in the SD card.
- The Real Time Clock and other timers & counters were also checked by comparing the time on the target under test with the time on the test rig PC.
- ARM exception handlers were written to output the value of the exception registers should exceptions occur during code execution.

All of the above tests and exception handlers output data were sent across both a CAN bus and a UART to a test PC that collated the information.

6.1.3 Test Rig Setup

The test rig setup is illustrated as shown below.

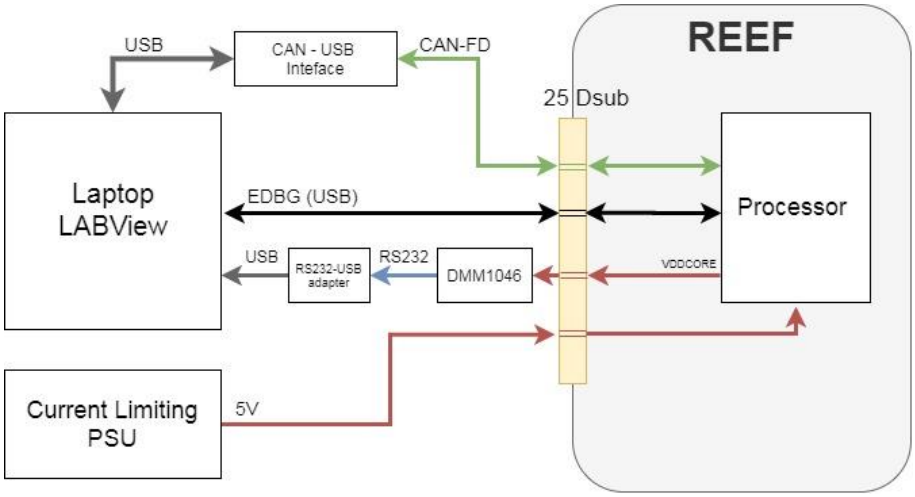

Figure 6: REEF Test rig setup

Test data was transmitted via two channels:

- A UART that the SAMV71 Xplained multiplexes into a USB channel using Atmels EDGB protocol.
- A Controller Area Network (CAN bus).

Two dissimilar communications channels were chosen in order to mitigate the possibility that the radiation dose affected one of these channels but not the rest of the chip under test. A test was also conducted of the CAN bus integrity (to ensure that the SAMV71 CAN controller was functioning correctly). This CAN test involved both transmission and reception of CAN data to and from the target.

Alongside the above tests, the current and voltage to the chip under test was monitored using a Digital Multi Meter (DMM).

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All of the above data was captured to a comma separated text file alongside the current radiation dose using a LABView program that interfaced to the DMMs, the CAN bus and the UART (through EDGB). The LABView program also incorporated a Graphical User Interface (GUI) that gave real time feedback to an operator. The GUI is shown below.

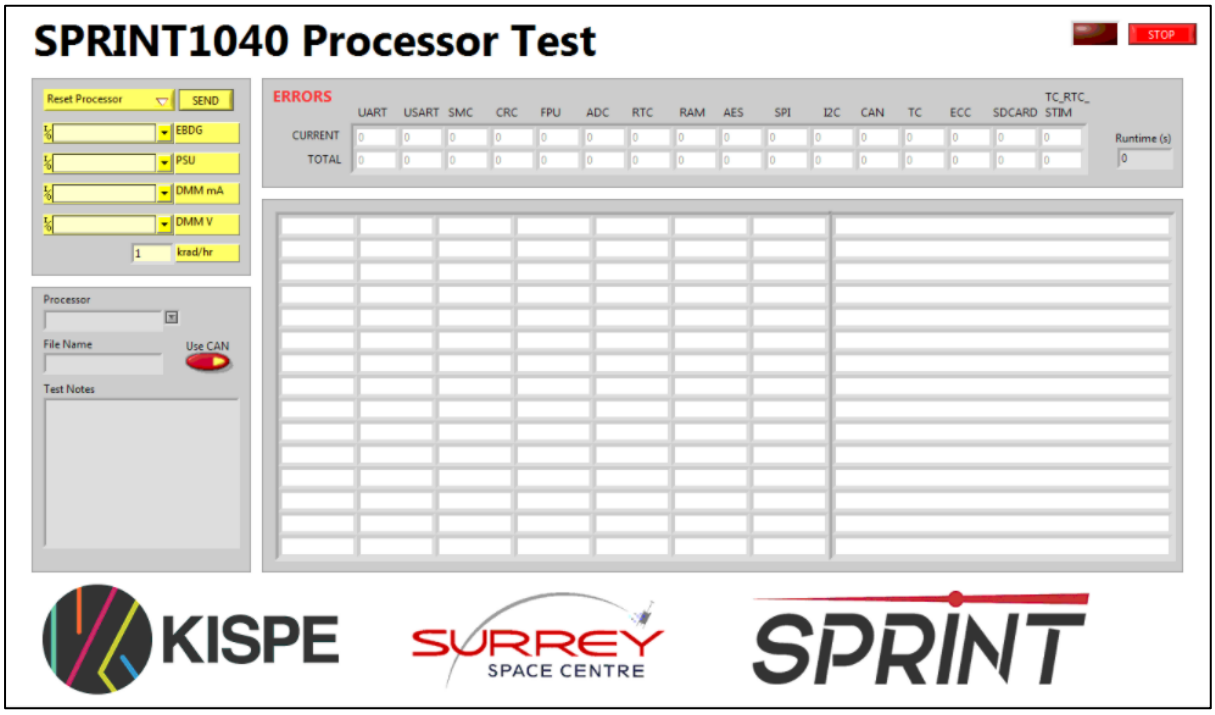

Figure 7: REEF Test Rig Utility GUI.

Testing was automated such that the system automatically attempted to resolve errors by resetting the peripheral causing the error using a stepped approach such as illustrated for the ADC test in Figure 8. This involved a combination of functions on the target (highlighted blue) and functions of the test rig utility (highlighted red). The number of failures were held in a non-volatile memory (SD card) such that the progression through the failures was maintained by the target through power cycles of the target.

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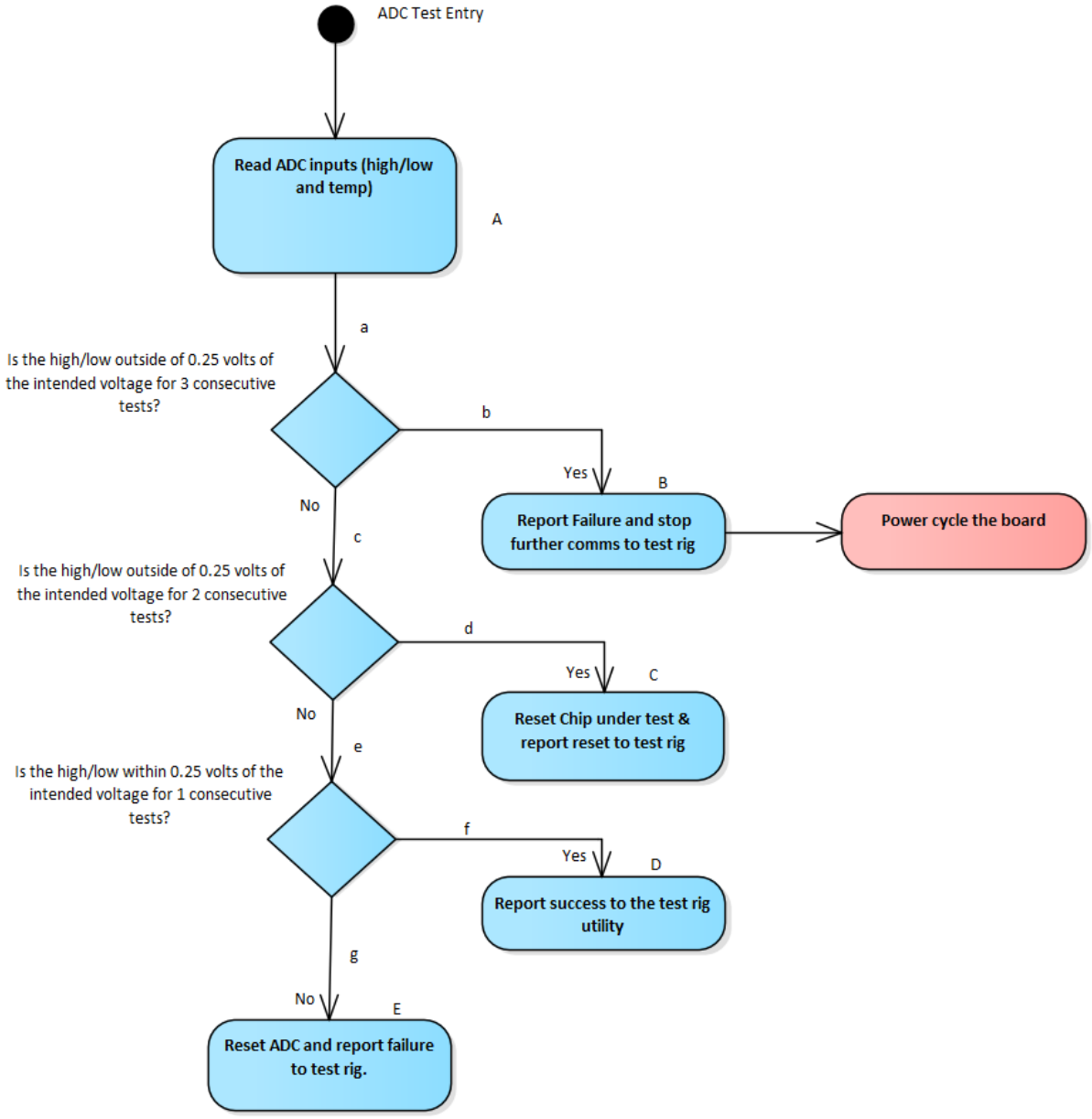

Figure 8: Automatic recovery from ADC errors

This mechanism allowed the tests to be conducted without operator interaction which allow the tests to run whilst being compliant with COVID-19 restrictions applied by the University of Surrey during 2020 and 2021.

6.1.4 Test Analysis

This section summarises the radiation environment calculations used to plan the experimental work for test board irradiations in REEF. The expected total ionising dose (TID) over the course of a nominal mission, and the dose rate within the test facility at the University of Surrey were calculated.

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6.1.4.1 ORBIT ANALYSIS

The Space Environment Information System (SPENVIS) was used for both the radiation environment specification (trapped protons, trapped electrons and solar protons) and the dose-depth calculations. The following inputs were used:

- 800 km sun synchronous orbit
- 10 year mission duration
- Standard trapped environment models AE8 and AP8
- SAPPHIRE solar proton model (at 90% confidence over 10 year mission duration)
- SHIELDOSE-2 used for dose-depth with planar shielding geometry
- Spacecraft shielding assumed to be 2mm

Trapped proton and electron fluxes in the Van Allen belts were calculated via SPENIVS using the standard AE8 and AP8 environment models. Figure 9 shows example integral flux maps above 2 MeV and 10 MeV for electrons and protons respectively.

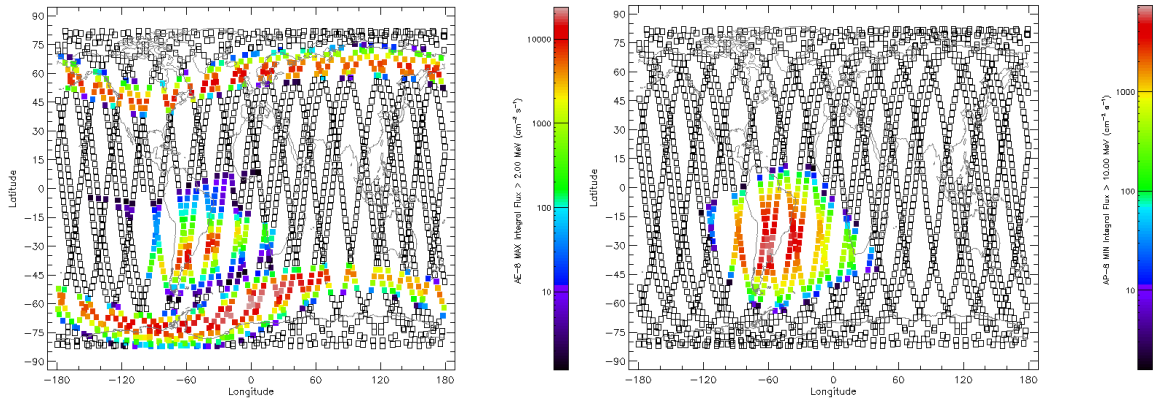

Figure 9: Integral flux maps for >2 MeV electrons (LHS) and >10 MeV protons (RHS) overlaid on a 800 km sun synchronous orbit trajectory.

Differential spectra from these calculations are shown in Figure 10. Also shown is a spectrum for solar energetic protons (SEPs) over the 10-year mission duration. As SEP occurrence is a probabilistic process, this spectrum is shown at the 90% confidence level (i.e. there is a 90% probability that the fluence will not be exceeded over this time frame).

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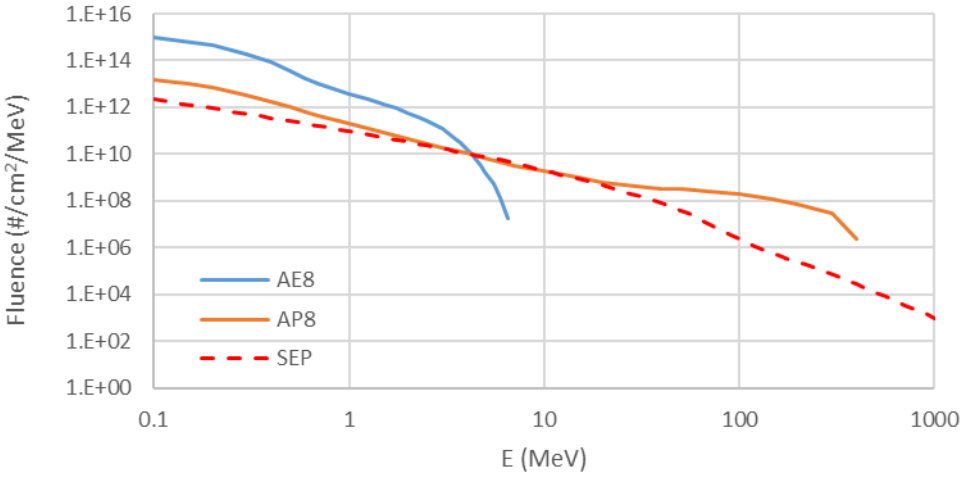

Figure 10: Differential electron and proton spectra for a 10 year period in 800 km sun synchronous orbit. Trapped spectra are shown for electron (AE8) and protons (AP8) and cumulative solar protons (SEP) calculated using the SAPPHIRE model are shown at the 90% confidence level.

Ionising dose as a function of shielding depth was calculated with SHIELDOSE-2 using the spectra shown in Figure 11. Planar shielding geometry was assumed as this is most suitable for locations that are relatively lightly shielded (at higher levels of shielding spherical geometry is more appropriate). It is clear from this plot that the influence of solar protons on dose is likely to be negligible for this environment – this is useful as it allows linear scaling of dose values for different mission durations.

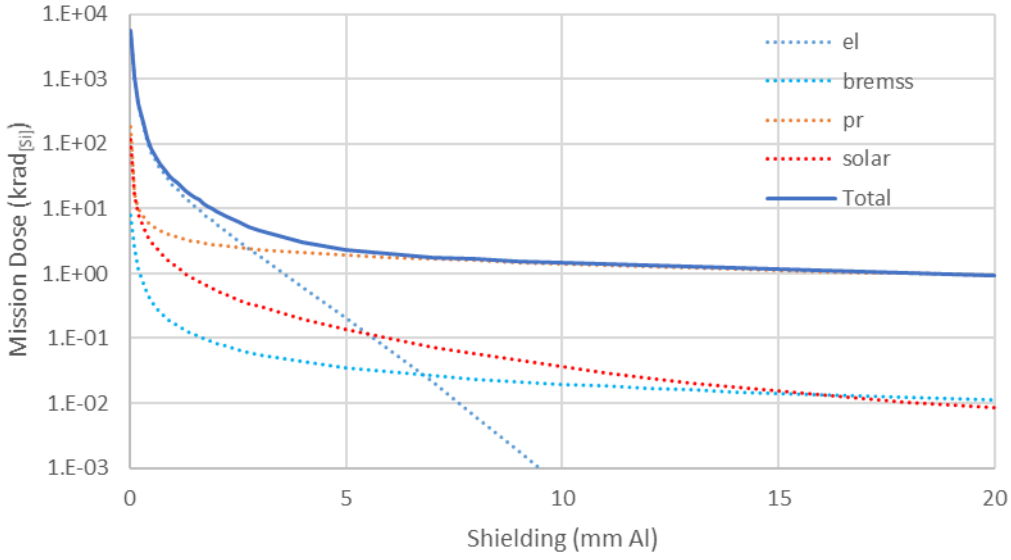

Figure 11: Ionising dose as a function of shielding depth (aluminium-equivalent) over the course of a 10 year LEO mission. A planar (slab) geometry is assumed. Contributing components ("el" = electron direct ionisation, "pr" = proton direct ionisation, "bremss" = Bremsstrahlung radiation and "solar" = SEPs at 90% confidence) are shown as dotted lines.

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For example, these calculations predict a total ionising dose of ~3 $kRad_{[Si]}$ over the 10 year LEO mission if 4 mm Al-equivalent shielding were assumed. The figure for 1 mm of Al-equivalent shielding is an order of magnitude higher at ~30 $kRad_{[Si]}$, and the figure for 2mm of shielding is 9 $kRad_{[Si]}$. The assumed level of spacecraft shielding is critical in determining the appropriate dose to evaluate the performance of candidate components.

6.1.4.1.1 REEF Calculations

Monte Carlo particle transport calculations were used to simulate a simple planar geometry whereby a 100 micron silicon sensitive volume is shielded by a 100 micron layer of fused silica (SiO_2) packaging material. The source itself is encapsulated with a thin layer of stainless steel attenuating the raw strontium-90 beta spectrum before incidence on the device under test. Figure 12 shows the raw and attenuated spectra alongside the additional (albeit small) attenuation due to component packaging. The estimated dose rate for an incident current of 1 pA/cm^2 (corresponding to a source-sample separation of approximately 9 cm) is ~1 $kRad_{[Si]}$ per hour. This dose rate could potentially be increased substantially by reducing the source-to-sample separation, however, as the strontium is (approximately) a point source, too high a dose rate could potentially introduce uncertainty due to anisotropy of the irradiation. It has been calculated that the micron layer thickness of the processor packages only makes a minor difference to the total TID and should be considered a minor risk.

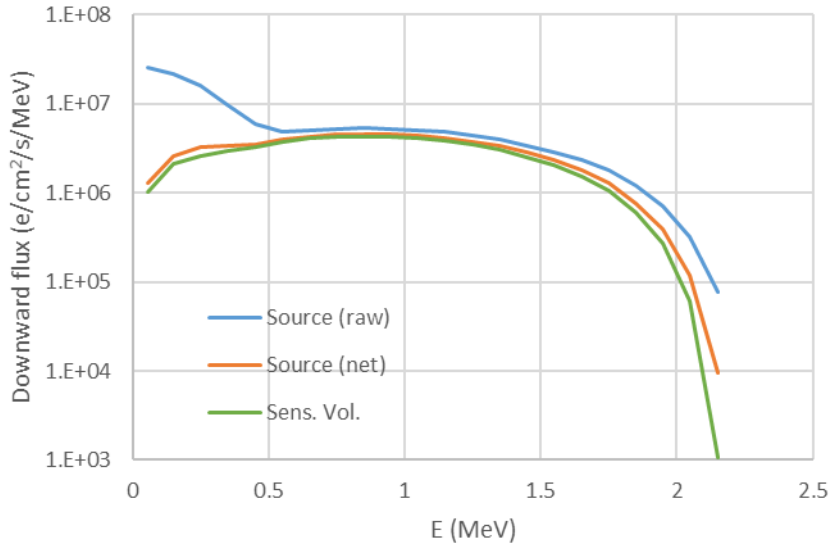

Figure 12: REEF electron spectra for the raw source (blue line), net source spectrum after encapsulation packing (orange line) and spectrum after nominal component shielding (green line). Although the impact of source encapsulation on the spectrum is clear, the impact of thin layers of component shielding is relatively small.

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6.1.4.1.2 Summary

Standard radiation environment tools were used to calculate the total ionising dose for a 10 year mission in 800 km LEO. The dose has a strong dependency on assumed spacecraft shielding, for example ranging from ~3 $kRad_{[Si]}$ to ~30 $kRad_{[Si]}$ for 4 mm and 1 mm Al-equivalent shielding respectively. In parallel the dose rate in REEF at a particular reference point for incident electron current (~1 $kRad_{[Si]}$ per hour) was calculated Therefore, based upon the specification of 2mm shielding, the expected dose will be ~9 $kRad_{[Si]}$. The conclusion was that the total mission dose could be achieved in REEF in a timescale of hours to tens of hours of exposure. Significantly higher and lower dose rates are achievable; however these are unlikely to be necessary unless it is desirable to expose devices under test to doses far in excess of the expected mission dose.

6.1.5 Test Plan

Given the above test analysis, the team decided to test four targets (from different manufacturing batches) to 10 kRad. This was considered the pass criteria for a 10 year, 800 km sun synchronous mission. Should time allow and the target survives this dose, the plan was to expose one of these four parts to as high a dose as was achievable before observing failures through the test rig utility.

6.2 SAMV71 Results

6.2.1 Overview

Boards Tested: 4/4

Batch Markings:

A. 1829YMH, Rev B, AAB
B. 1813C A44HUA, Rev B, AAB
C. 1745C A483RA, Rev B, AAB

Board	Batch	Test Time (hrs)	TID (kRad)	Start Voltage (V)	End Voltage (V)	Start Current (mA)	End Current (mA)	NOTES
1	A	14.45	14.45	3.281	3.281	72.69	73.95	1 kRad/hr dose rate No Failures Timer Errors at Midnight, but these were expected. See 6.2.4.1
2	B	15.5	15.5	3.279	3.282	74.93	75.21	1 kRad/hr dose rate No Failures Timer Errors at Midnight, but these were expected
3	A	5.0	10.00	3.271	3.272	74.05	74.34	2kRad/hr dose rate No Failures NOTE: At this point, KISPE and SSC decided to

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								increase the dose rate since the devices are affected by the total dose and not specifically the dose rate. This decreased the test time.
4	C	47.5	95	3.275	3.275	73.79	74.24	*Destruction Test* 2 kRad/hr dose rate Testrig Bluescreened twice during test due to USB driver compatibility with Windows 7. Data for 0->35k, 60k and 95k All tests passed at 60k. ECC flash degrading at 95k. Self-correcting single bit errors

6.2.2 Evidence Files

Board 1: V71 Board 1 REEF.txt

Board 2: V71 Board 2 REEF.txt

Board 3: V71 Board 3 REEF.txt

Board 4: V71 Board 4 REEF.txt, Board 4 Part (*2-4*).txt and V71 Annealing.txt

These raw data files are available by request to the OSSAT team. We are happy to supply this information but it needs to be supplemented with a format description.

6.2.3 Error Recovery Actioned

Board	Error Recovery Steps Actioned	Results
1	Real time Clock and Timer/Counter errors observed at cross over through midnight.	RTC error recovery actioned and timers resynced to testrig TC error recovery actioned and timers resynced to testrig
2	Real time Clock and Timer/Counter errors observed at cross over through midnight.	RTC error recovery actioned and timers resynced to testrig TC error recovery actioned and timers resynced to testrig
3	None	N/A
4	The Flash memory CRC check began to fail triggering an automatic reset of the chip that sometimes resolved the	All CRC error recovery steps actioned. Power cycles intermittently corrected the errors,

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	problem. These errors became increasingly frequent as the dose became larger.	

6.2.4 Observed Failures/Recoveries

6.2.4.1 Midnight Timer Rollover

When testing the RTC timers, the test rig compares the times received from the target to its own RTC value. This comparison is done by converting the time strings into numeric timestamps and subtracting the values to see if the difference is greater than the specified 10 secs of the test. However, the rig's own numeric timestamps are a count from 0 at midnight, upwards in seconds. When the test of boards 1 and 2 ran over midnight, the targets RTC counts rolled over as midnight passed (in the thousands), whereas the test rig's timestamp was reset to 0 for the new day. This resulted in a reported 'ERROR' of both the TC and RTC values on the target, however this was just a quirk of the test rig setup. These errors were therefore discounted as it was known and expected behaviour. On both occasions, the test rig sent the commands to reset the timers of the target and they both successfully re-synced back together for the remainder of the test without further errors.

6.2.4.2 Flash Error Correction Code (ECC)

The only notable failure on any of the 4 boards was that of the ECC during the destruction test. In this test, every test was reporting successful 'OK' results up and until 60 kRads TID. At this point, the data stream was lost due to a test rig operating system crash. When the test rig was restarted, the board was up to 95 kRads. At this point, intermittent errors were being reported in the Flash memory ECC. Unfortunately due to the data loss, it is not known exactly at what TID the ECC errors began, only somewhere in the range from 60 to 95 kRads. The errors reported were indicating problems with the flash memory, where single bits were being corrupted. However, these errors were being corrected by the ECC hardware, resulting in the read and write data matching correctly. This generated error messages of the following type:

'10:05:03,,ECC,ERROR,WRITE SUCCESS - READ SUCCESS - Unique Error on LSB - READ DATA MATCHES'

Above 95 kRads, these errors became frequent to the point where power cycles were only occasionally able to resolve the problem until testing was stopped at 100 kRads. Throughout this period, the ECC hardware detected failures in the underlying Flash hardware. All failures were corrected by the ECC.

Since the target had proven on four occasions to be resilient to the pass criteria of 10 kRad dose of radiation, the team decided that the exact point that the chip failed was not significant. The results indicate that the SAMV71 begins to fail somewhere between 60 and 95 kRads.

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6.2.5 Annealing Post Destruction Results

An annealing test was conducted at 72 hours (post weekend) after removing Board 4 from REEF at the end of the destruction test, to see if the reported ECC errors in the flash memory would correct and successful report 'OK' again. As noted above, the board was exposed to 100 kRads during the test.

The test saw a slight improvement in the frequency of the intermittent Flash memory failures, with these occurring less often than during the TID test. However, the 'Unique error on LSB' was still reported frequently, indicating there were no major changes to the processor's performance after 72 hours.

6.2.6 Current Consumption Observations

6.2.6.1 Warm Up

Across all the boards, the SAMV71 shows a reduced current for the first few test loops and then increases to a nominal value after this, most likely related to the temperature of the processor. For example, for Board 4 there was an increase from 70 mA to 73.8 mA

6.2.6.2 10 kRad Mission Duration

Board 3 of the SAMV71 was tested to a 10 kRad TID, matching the specification set out by the OSSAT team. Figure 13 shows the minimal increase in current over the test, using the RAM test as the example. Figure 14, Figure 15 and Figure 16 show the current consumption across different tests, with Figure 14 showing memory type tests, Figure 15 the interface tests and Figure 16 the timer tests. On the SAMV71 the CRC and the FPU use the most power, of the memory tests, and the UART and USART use the most power of the interface tests.

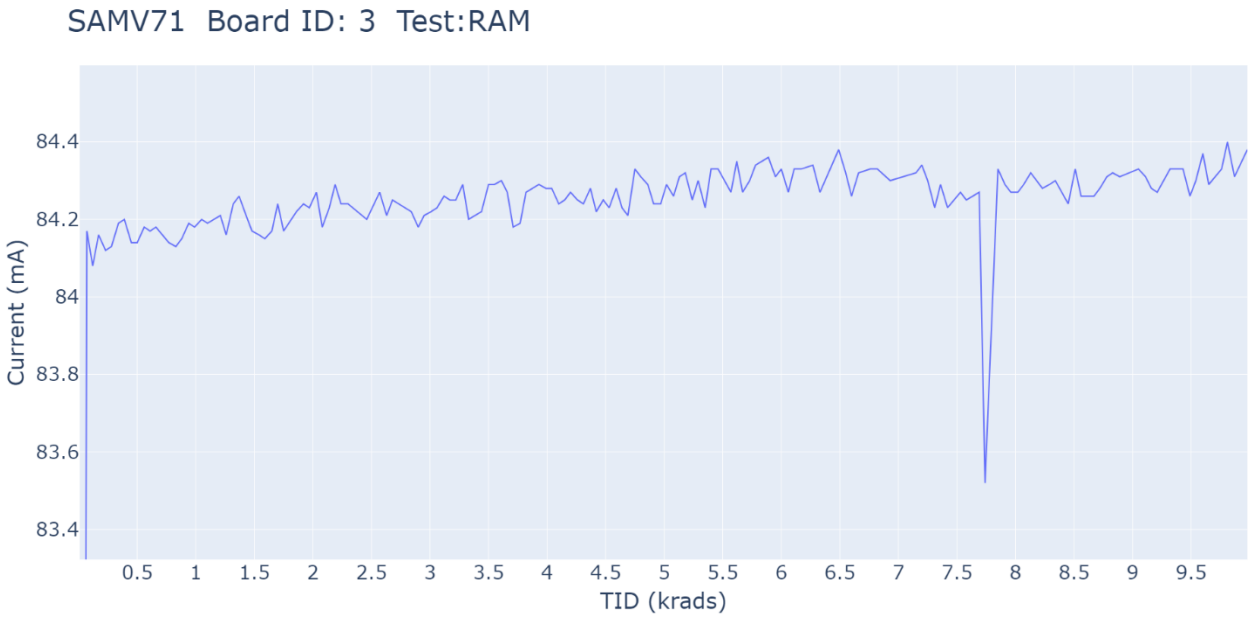

Figure 13: SAMV71 current consumption by the RAM test up to 10 kRads TID

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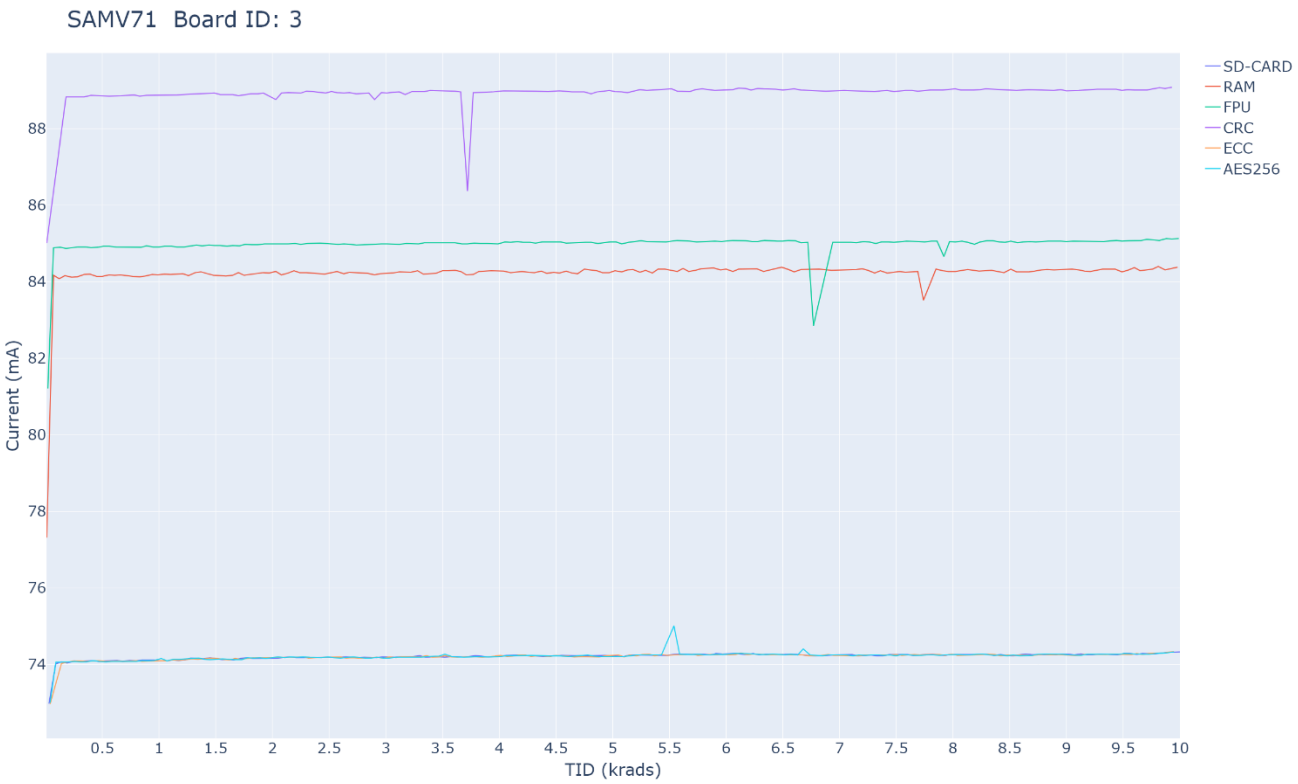

Figure 14: Comparison of current consumption of each of the different memory tests up to 10 kRads on the SAM71. The ECC, AES and the SD-CARD all have identical current consumption, hence only the AES is visible on this plot.

Figure 15: Comparison of current consumption of each of the different interface tests up to 10 kRads on the SAM71. The UART and USART draw the most current, CAN the least. After a TID of 10 kRads, the processor was drawing 0.3 mA more current when running each interface test.

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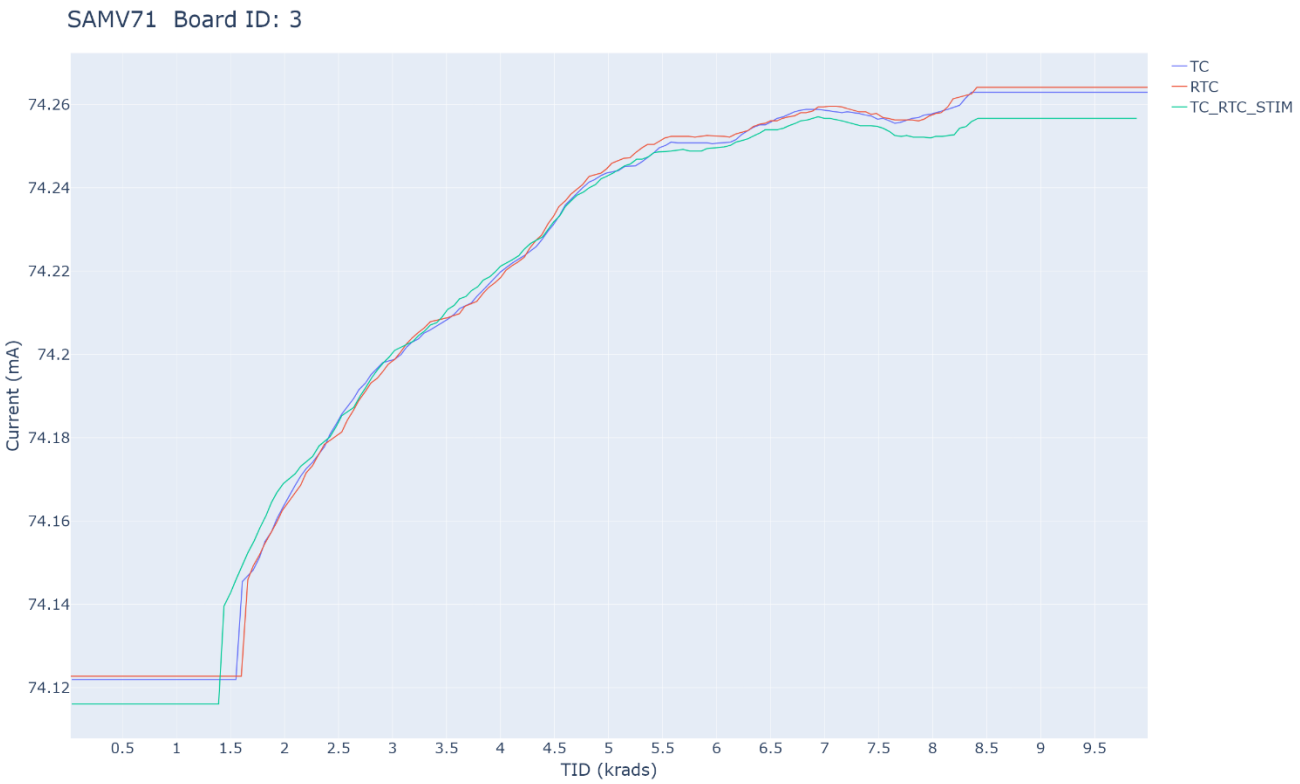

Figure 16: Comparison of current consumption of each of the different timer tests up to 10 kRads on the SAM71

6.2.7 Destruction Test

As seen in Figure 17, the overall current increase throughout the destruction test for SAM71 was minimal, increasing from a starting value, on the USART test, of 73.8 mA after warmup, to 74.3 mA at 97 kRads. The data gaps, caused by test rig failures, are marked by two green lines in Figure 17, with the first gap at 35 to 59 kRads and the second at 61 to 94 kRads. For the last period of the test, above 94 kRads, the board struggled to restart correctly or complete a full test run, which can be seen by the large variation in USART currents. At 94 kRads, the board was not able to initialise and begin running continuous loops reliably, so the nominal current value reduced to the original starting value after periods of inactivity prior to a power cycle for loss of UART EDBG comms.

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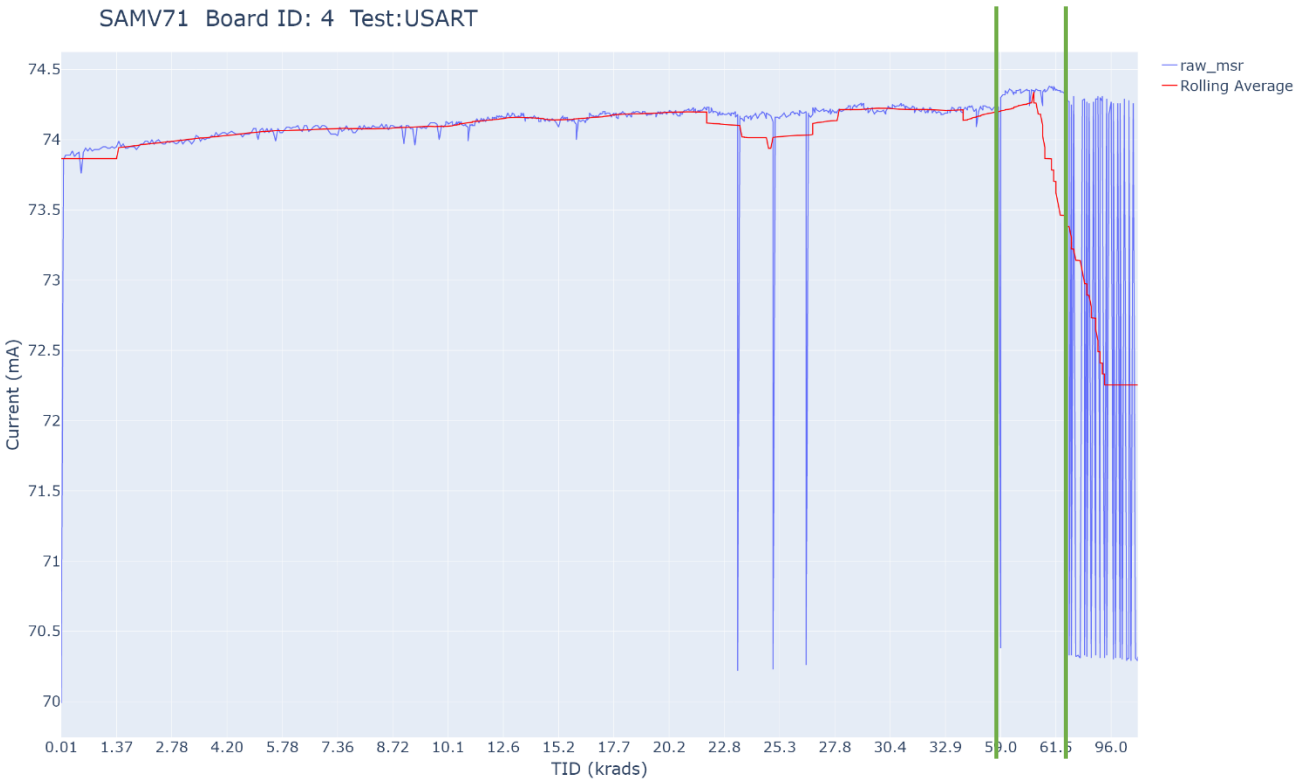

Figure 17: Current consumption for SAMV71 destruction run, for the USART tests. Note: The green vertical lines indicate gaps in the data, due to testrig failures.

6.3 Processor Performance

6.3.1 Test Setup

The OSSAT team is aware that major performance issues occur in relation to writes to a file system. Therefore, in order to assess performance, software was integrated as shown in Figure 18.

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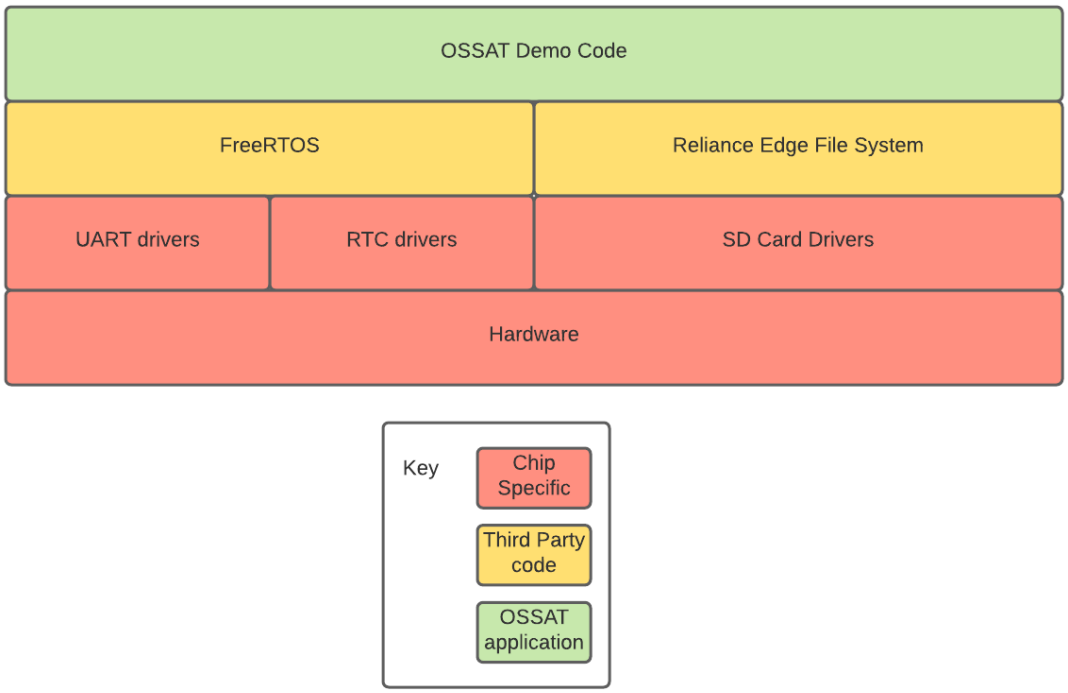

Figure 18: OSSAT SAMV71 file system performance

FreeRTOS was selected because of its strong, open source community, small memory footprint and general simplicity.

The Reliance Edge File System was selected because it is open source and is designed to work reliably following sudden power loss during a commit.

A worst case scenario for platform software file writes was estimated. This resulted in a worst case burst requirement of 6800 bytes across 12 different files in 50ms.

Tests were performed with and without the processor's cache enabled. The feature size of cache means that it is often the weakest part of the chip with respect to single event upset and is therefore often disabled. The SAMV71 has some ECC protection of its cache and therefore, there was interest in understanding the effect of enabling and disabling the cache memory.

6.3.2 Test Results

Tests were run 10 times, writing data to 12 files from 12 different FreeRTOS tasks. This involved the file write and a "red_transact()". This "red_transact()" commits the change to the underlying media (an SD card was chosen). Therefore, the burst requirement of 50ms applies to the file write time only. See section 7 for conclusions.

6.3.2.1 Release build with cache disabled

File write max time: 16.51ms

File write average time: 13.67ms

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File write std dev: 1.6ms

red_transact() max time: 95ms

6.3.2.2 Release build with cache enabled

File write max time: 9.6ms

File write average time: 7.75ms

File write std dev: 0.86ms

red_transact() max time: 88.4ms

7 Conclusions

From the limited testing performed on the SAMV71, it remains a candidate OSSAT processor, both from a performance and radiation tolerance perspective. Further work is needed to validate this further.

It is capable of writing to files at a speed which is fast enough for the needs of the OSSAT platform requirements (with cache enabled consuming approximately. 20% of the processor's processing run time under worst case burst write conditions).

It is also capable of withstanding significant TID without failure. Through analysis, a 10 year 800km sun synchronous orbit would equate to approx. 10 kRads of radiation dose. Under the destruction test, the chip only began to fail somewhere between 60 and 95 kRads. The current increase observed was also negligible.

8 Future Work

Further work is required in order to derisk the SAMV71 as a suitable processor for the OSSAT platform. The OSSAT team are therefore planning the following:

8.1 SEU/Latch-up testing

The OSSAT team have a test plan drafted for a proton irradiation test campaign to test for tolerance against the Single Event Upset and Latch up effects.

8.2 Further performance testing

The design goal is to develop an AOCS system capable of running AOCS loops at up to 12Hz. This would form a major performance requirement on the SAMV71 processor. Therefore, a further task would be to develop representative AOCS software that would exercise the processor and assess its suitability to this task.

9 Credits

Many thanks to Research England and SPRINT for supporting this project, to the University of Surrey for their contribution and to the growing and amazing collaborators who make up the OSSAT team. This includes Dr Keith Ryden, Dr Benjamin Clewer, Dr Alex Hands, Jamie Bayley, Dr Chris Bridges, Dr John Paffett, Paul Madle Anita Bernie, Angela Brown, Mauricio De Carvalho and Ian James.

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10 Appendix A

The ARM Cortex M7 core incorporates ECC protection on its instruction and data cache that recovers from errors. The following table shows how different types of cache RAM are protected:

RAM type	Protection	Recoverable error	Non-recoverable error	Hard error support
Data tag RAM	SEC-DED ECC	Error seen as single bit errors	Error seen as a multiple bit error	Up to two hard errors
Data cache data RAM	SEC-DED ECC	Error seen as single bit errors	Error seen as a multiple bit error on dirty lines	
Instruction tag RAM	SEC-DED ECC	Any error, single or double, on the tag or valid bit stored in the RAM	None[a]	
Instruction cache data RAM	SEC-DED ECC	Any error on the data stored in the RAM	None[a]	

a. The instruction cache is never dirty so cache RAM errors are always recoverable by invalidating the cache and retrying the instruction.

Figure 19: Cortex M7 ECC features

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